LINEAR AND DIGITAL SEMI-CUSTOM IC DESIGN PROGRAMS

Introduction

This semi-custom IC design brochure contains a complete outline and summary of Exar's unique semi-custom IC design, development, and production program and capabilities. This technique, which was pioneered by Exar, offers a unique and effective method of manufacturing an almost unlimited variety of custom linear or digital monolithic IC's with greatly reduced cost and development times. Exar makes this possible by stocking wafers that are completely fabricated except for the final process step of device interconnection which metallizes all selected components together in the required circuit configuration. This enables an engineer to design a metal mask based on his circuit which will interconnect "uncommitted" components on the prefabricated wafers.

The semi-custom program, is intended for those customers seeking cost-effective solutions to reduce component count and board size in order to compete more effectively in a changing marketplace. The program allows a cutomized monolithic IC to be developed with a turn-around time of several weeks and at a small fraction of the cost of a full custom development program.

Exar's semi-custom design programs cover both the conventional bipolar as well as the integrated injection logic (I^2L) technologies. In each of these technology areas, Exar has developed a number of monolithic semi-custom chips, called "Master Chips." This brochure reviews the features and the capabilities of these Master Chips to enable the user to choose the right chip for his semi-custom program.

EXPERIENCE AND PRODUCTS

Since the introduction of the semi-custom technology by Exar in 1971, we have successfully designed or completed over 300 semi-custom IC products which cover a wide range of applications and a very broad customer base. However, Exar's experience and expertise in the area of bipolar and I^2L technologies extend well beyond semi-custom designs to a wide range of standard IC products. Today Exar has one of the most complete product lines of IC oscillators, timing circuits and phase-locked loops. In the field of industrial control circuits, Exar manufactures a broad line of quad and dual operational amplifiers, remote-control and servo driver IC's and power control circuits.

EXCELLENCE IN ENGINEERING

Exar quality starts in Engineering where highly qualified people are backed up with the advanced instruments and facilities needed for design and manufacture of custom, semi-custom, and standard integrated circuits. Exar's engineering and facilities are geared to handle all three classes of IC design: (1) semi-custom design programs using Exar's bipolar and I^2L master chips; (2) full-custom IC design; (3) development and high-volume production of standard products.

Some of the challenging and complex development programs successfully completed by Exar include analog compandors and PCM repeaters for telecommunication, electronic fuel-injection, anti-skid braking systems and voltage regulators for automotive electronics, digital voltmeter circuits, 40 MHz frequency synthesizers, high-current and high-voltage display and relay driver IC's, and many others.

NEW TECHNOLOGIES

Through company sponsored research and development activities, Exar constantly stays abreast of all technology areas related to changing customer needs and requirements. Exar has recently completed development efforts in Integrated Injection Logic (I^2L) technology, which offers unique advantages in the area of low-power, high-density logic arrays. Exar has a complete design engineering group dedicated to this new technology, and is currently supplying over thirty different custom and semi-custom I^2L products.

FIRST IN QUALITY

From incoming inspection of all materials to the final test of the finished goods, Exar performs sample testing of each lot to ensure that every product meets Exar's high quality standards. Exar's manufacturing process is inspected or tested in accordance with its own stringent Quality Assurance Program, which is in compliance with MIL-Q9858A. Additional special screening and testing can be negotiated to meet individual customer requirements.

Throughout the wafer fab and assembly process, the latest scientific instruments, such as scanning electron microscopes, are used for inspection, and modern automated equipment is used for wafer probe, AC, DC, and functional testing. Environmental and burn-in testing of finished products is also done in-house. For special environmental or high reliability burn-in tests outside testing laboratories are used to complement Exar's own extensive in-house facilities.

FIRST IN SERVICE

Exar has the ability and flexibility to serve the customer in a variety of ways from wafer fabrication to full parametric selection of assembled units for individual customer requirements. Special marking, special packaging and military screening are only a few of the service options available from Exar. We are certain that Exar's service is flexible enough to satisfy 99% of customer needs. The company has a large staff of Applications Engineers to assist the customer in the use of the product and to handle any request, large or small.

June 1979

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Semi-Custom Design Concept

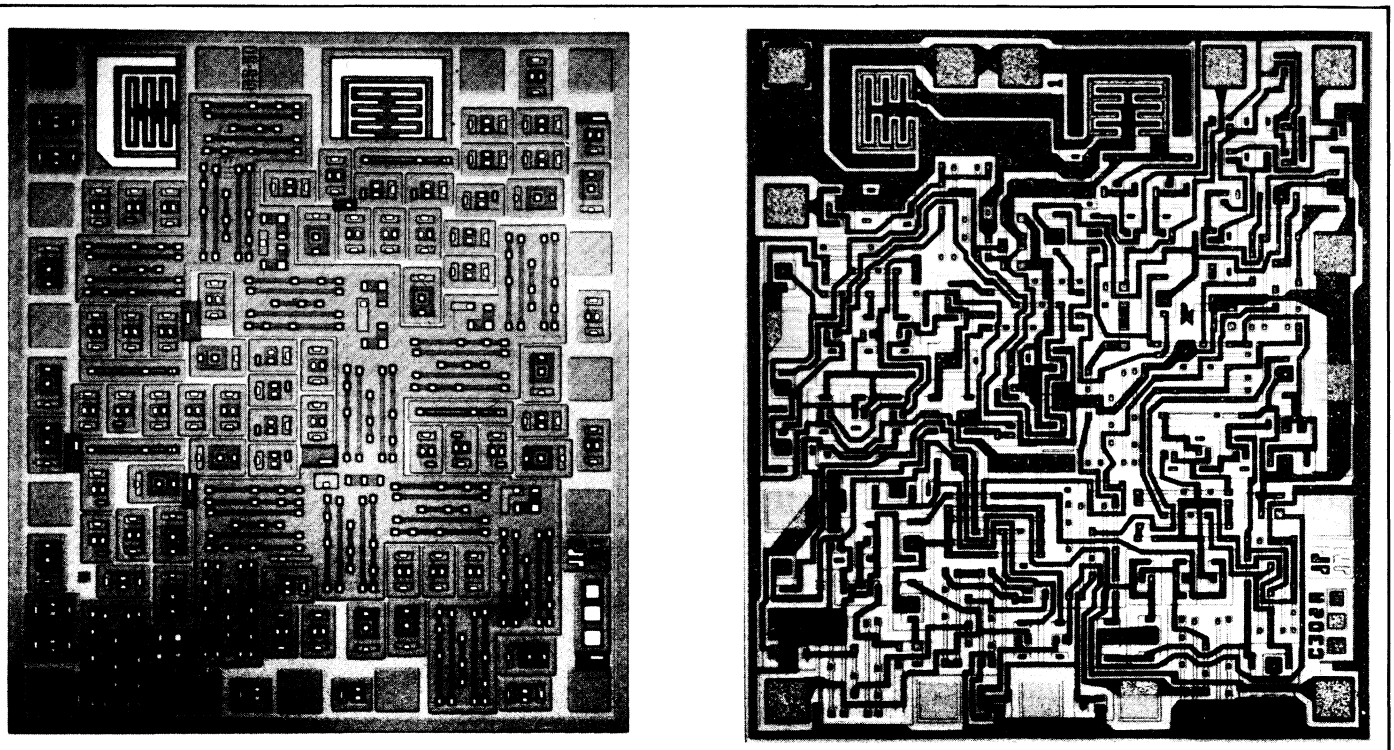
Traditionally, the development of custom IC's has been a long and costly undertaking: the development time would normally run in excess of one year; design changes are slow and costly, and it may take a long time to get from prototype to full production. Because of these difficulties, the use of custom IC's could be economically justified only when a very large quantity of circuits, i.e., several hundred-thousand or more units, were required during the life of the end product. In the past, these drawbacks have severely limited the use of custom monolithic IC's.

The semi-custom design concept, pioneered by Exar, now overcomes this traditional problem. Exar makes this possible by stocking wafers that are completely fabricated except for the final process step of device interconnection which metallizes all selected components together in the required circuit configuration. This enables an engineer to design a metal mask based on his circuit which will interconnect the *uncommitted* components on the prefabricated wafers, and thus convert them into *customized* chips corresponding to the customer's design. This unique method of IC design and development allows one to develop an almost unlimited variety of custom linear or digital integrated circuits at very substantial cost savings.

The semi-custom program, is intended for those customers seeking cost-effective solutions to reduce component count and board size in order to compete more effectively in a changing marketplace. The program allows a customized monolithic IC to be developed with a turn-around time of several weeks, at approximately 10% to 20% of the development of tooling costs associated with the conventional full custom designs. The semi-custom design concept is an interactive or co-operative development effort between Exar and the customer. In most cases, the cost and the development time for the program can be reduced even further by having the customer do the design and breadboarding of his own semi-custom IC, using Exar's Design Kits, instruction manuals and layout sheets.

The semi-custom design approach is based on a number of standardized IC chips with fixed component locations. These standardized IC chips, called Master Chips, contain a large number of *undedicated* active and passive components (i.e., transistors, resistors, logic gates etc.). These integrated components can be interconnected in thousands of different ways, with a *customizing* interconnection pattern. Each different metal interconnection pattern creates a new custom IC. The figures below show the magnified photograph of such a Master Chip both at its *prefabricated* form, and after its customization with a special interconnection pattern, which converts it to a completed custom chip. This method is called *semi-custom*, rather than *full custom* since only the last layer of tooling is changed to customize an IC chip, and the rest of the layers are standard. As a result, the development phase is very short, far less expensive and risk free, compared to conventional full- or dedicated-custom IC's. Similarly, if a design change or iteration is necessary, it can be readily accommodated, within a matter of weeks, by simply generating a new or modified interconnection pattern.

Exar offers a wide choice of Master Chips for linear and digital semi-custom design: At present there are five bipolar Master Chips aimed primarily for linear design, and three I^2L Master Chips for digital or analog/digital LSI design. Additional chips are under development for a variety of special applications. The details of each of these chips are discussed further in the later sections of this brochure.



Magnified Photograph of a Linear Master Chip, Before and After Customizing

SEMI-CUSTOM DESIGN KITS

Exar offers *two* semi-custom "Design Kits," one intended for linear or analog circuits, and the other for digital designs. The linear design kit is based on Exar's bipolar linear IC design and fabrication technology. The digital design kit is derived from Exar's integrated injection logic or I^2L technology. Each of these kits contain a comprehensive instruction manual, a set of layout sheets and a large number of monolithic circuit components or "kit parts" which consist of transistor and resistor arrays and logic subblocks. This provides the design engineer with the ability to evaluate and characterize his design using the same "breadboarding" techniques as used in conventional (i.e., non-integrated) designs. Except, in this case, monolithic IC kit parts are used for the critical circuit components. Since these kit parts exhibit electrical characteristics which are nearly identical to those on the final monolithic IC, they provide an accurate simulation of the final circuit performance during this breadboard analysis stage. Once the breadboard evaluation is satisfactorily completed, he can then proceed to do his own IC layout using the layout sheets and the instructions included in the Design Manual supplied as a part of the Kit.

Semi-custom design is a straight-forward technique: it is basically no more than simply interconnecting a number of prefabricated circuit components on a monolithic chip. In this sense, it is similar to conventional printed circuit board layout once the circuit is designed, breadboarded and evaluated for "worst-case" component tolerances. The availability of a complete Design Kit allows the customer the choice of designing his own semi-custom IC, in consultation with Exar, and then submit Exar a completed pencil layout of his circuit, on the appropriate Master Chip overlay. Exar would then review this layout for feasibility and accuracy and proceed to generate the necessary final tooling to customize the monolithic chip. This "interactive" design approach where the customer can do his own design and layout using one of Exar's Design Kits can save significant development cost and time. These Design Kits also provide an excellent training aid for circuits and systems designers in familiarizing themselves with the basics of monolithic IC design.

YOUR FIRST STEP

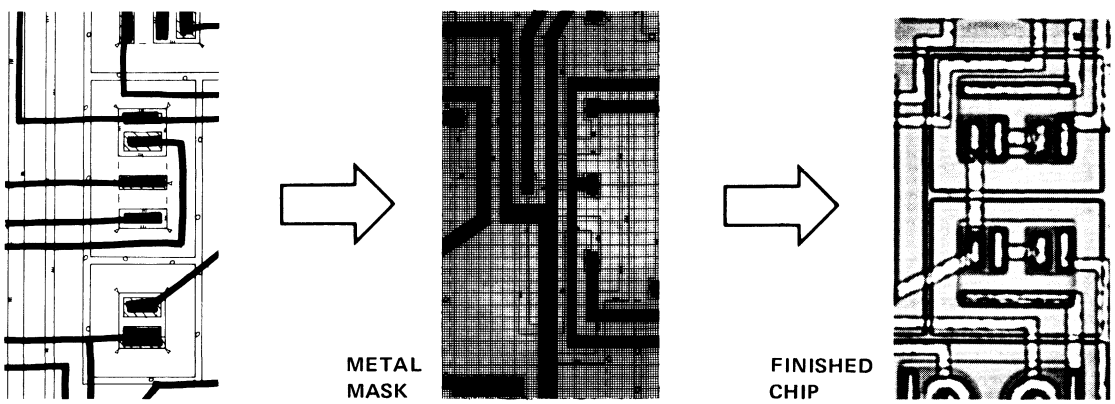
Your very first step, at the start of the semi-custom program, should be to contact Exar for a preliminary analysis and discussion of your needs. This can be done even while the program is still at the "thought stage." This initial review by Exar is performed at no cost to the customer. Yet it is essential to the success of the program since it avoids any possible design pitfalls or misunderstandings. This early interaction also allows you to find out some of the options or variations available in Exar's semi-custom programs and choose the one which is best suited to your needs.

The following is a typical check list of items and information which is required by Exar's technical staff to provide you with an accurate feasibility study of your project along with a budgetary estimate of the development costs, time tables and production pricing.

- A block diagram of circuit function, and input/output interface requirements.
- A circuit schematic or logic diagram of your circuit.
- Preliminary or objective performance specifications, limits on critical circuit parameters (also possible tradeoffs which may be allowed).
- Types of electrical testing required for production units (i.e., AC or DC parametric testing, functional testing etc.).
- Production quantity requirements.
- Desired development and production time tables.
- An indication of how much of the breadboarding, layout etc. can be done by you the customer, using Exar's Design Kits.

Once the above data package is submitted to Exar, we would review it and respond to you with a feasibility assessment and a budgetary cost and price estimate for your semi-custom program, within a few days after the receipt of the above information package.

STEPS OF SEMI-CUSTOM DESIGN



Answers to Frequently Asked Questions

Based on our long experience with Exar's bipolar and I^2L semi-custom Master Chips, we have compiled a comprehensive glossary of the "most often asked questions" concerning the program. The following is a list of these questions and their answers:

WHAT IS THE COST OF THE BASIC PROGRAM?

The cost of the semi-custom development program depends on how much of the design and the layout is done by the customer, using Exar's design kits. In general, the "basic" semi-custom program where the customer does the design, breadboard evaluation and the pencil layout on the Master Chip worksheet, and Exar only does the IC tooling and the prototype fabrication, is the most economical and cost effective approach.

In the case of the bipolar semi-custom designs, the development cost for the basic program is in the range of $3,000 to $5,000, starting with an accurate layout supplied by the customer. The above prices also include the cost of 50 monolithic prototypes delivered at the completion of the program. Additional prototypes are available at a nominal cost, in minimum lots of 200 units.

In the case of the I^2L semi-custom designs, the basic development program costs are in the range of $5,000 to $10,000, depending on the layout complexity and the particular Master Chip used. This development cost also includes 25 monolithic prototypes. Additional prototypes are available at a nominal cost, in minimum lots of 100 units each.

WHAT IS THE DEVELOPMENT TIME?

Typical development time for the basic bipolar semi-custom program is *six* to *eight* weeks, starting with the customers pencil layout and ending with the monolithic prototypes. If Exar is required to do the IC layout or breadboard evaluation, several additional weeks may be required to complete the development program.

In the case of I^2L semi-custom development programs, typical development time is *eight* to *fourteen* weeks, starting with the pencil layout on the Master Chip worksheet. The I^2L semi-custom program takes slightly longer than bipolar because it requires three layers of custom tooling, rather than one, to customize a prefabricated Master Chip.

WHAT IF ADDITIONAL DESIGN CYCLES ARE NEEDED?

Upon evaluation of the initial prototypes, if the customer desires to modify the design or the layout, a new design iteration cycle can be completed within *five* weeks for the bipolar designs, and within *eight* to *ten* weeks for the I^2L designs.

Typical costs of additional design cycles are $2,000 to $3,000 for bipolar designs and $3,500 to $5,000 for I^2L designs. These costs also include the additional prototypes supplied at the completion of the design interation cycle.

WHAT ABOUT PRODUCTION PRICING?

The production pricing of monolithic IC's depend on a number of important factors such as:

a) Circuit complexity (i.e., yield)
b) Device performance and test requirements
d) Special environmental screening requirements (burn-in, hermeticity tests etc.)
e) Package type required

In the case of a custom IC, it is impossible to anticipate the impact of these factors in advance, since each custom IC by definition, has some unique requirement or feature associated with it. After reviewing your specific needs, particularly with regards to the circuit performance and the quantity requirements, Exar can provide you with a detailed proposal outlining the cost breakdown and the production pricing for your particular circuit.

WHAT ABOUT TESTING OF SEMI-CUSTOM IC'S?

The initial monolithic prototypes supplied to the customer at the conclusion of the basic semi-custom program are not electrically tested. However, upon evaluation of these prototypes and the definition of test specifications by the customer, Exar can develop test software and fixtures to provide fully tested production IC's. All production devices receive 100% electrical test and screening to a mutually agreed upon device specification. In addition to the complete electrical testing, all of the production devices are screened by Exar's Quality Assurance Department to assure compliance with the agreed-upon Acceptable Quality Level (AQL) Standards.

There is normally a non-recurring engineering charge associated with this test system generation, to cover the cost of the test fixture and the computer software development. Depending on the complexity of the test requirements, this test-engineering charge is normally in the range of $1,000 to $4,000.

Exar can perform two basic types of tests for production IC's: (1) parametric testing which measures a specific parameter value (normally current or voltage) and compares it against pre-established limits; (2) functional testing which applies a series of operating conditions and compares the circuit under test with a known good device. These two types of tests can be performed both as steady state (DC) or dynamic (AC) measurements. Although DC tests are easily implemented by automated testers, AC tests are usually difficult and expensive to perform in production.

Test system development cost is not included in the basic semi-custom development program. This development effort usually requires *four* to *six* weeks to complete, and is normally not initiated until the evaluation and the approval of the initial IC prototypes. However, if a definite production commitment is made at the commencement of the semi-custom development program, the test system development effort can be initiated in parallel with the chip development effort. Exar has a complete computer-controlled IC test facility, and offers complete IC testing capability for production units. A detailed description of Exar's test capabilities are given in page 9).

WHAT PACKAGE TYPES ARE AVAILABLE?

All semi-custom IC's are available in dual-in-line (DIP) packages. Commercial grade units are normally packaged in plastic DIP packages. Exar offers a wide selection of such packages, in 8-, 14-, 16-, 18-, 20-, 24-, 28- and 40-pin versions.The industrial on military grade products requiring hermetic packaging are available in frit-seal ceramic (CERDIP) packages. All of the packaged units are subjected to Exar's stringent quality assurance specifications prior to shipment (see pages 36 and 37).

IS THERE A SECOND-SOURCE FOR SEMI-CUSTOM IC'S?

In most high-volume production applications of IC's, the customer often requires more than one supplier of a given IC. Anticipating this "alternate-source" requirement, Exar has made contractual agreements with other IC manufacturers to provide a second-source for many of Exars semi-custom IC'S.

In addition, Exar's XR-A100, XR-B100, XR-D100 and XR-F100 family of bipolar Master Chips are direct replacements for the "Monochip A, B, D and F" products manufactured by Interdesign, Inc. of Sunnyvale, California.

In certain cases, where a critical supply situation may exist, Exar can also provide a special "bonded inventory" of parts, either in chip form or in packaged form, with prior arrangement with the customer.

WHAT IF MY PRODUCTION REQUIREMENTS EXCEED MY INITIAL EXPECTATIONS?

It is not unusual for an end-product using the semi-custom IC to be extremely successful in a very short time. In that case, the anticipated volume of the custom IC may jump from few thousand units to several hundred -thousand units. When that happens, Exar can quickly convert your semi-custom design to a full custom chip and make it much more cost-effective for you. Translating a semi-custom design to a full custom IC is a very simple trouble-free step, which can be normally done in *less than six months* (see page 7) and at a modest cost.

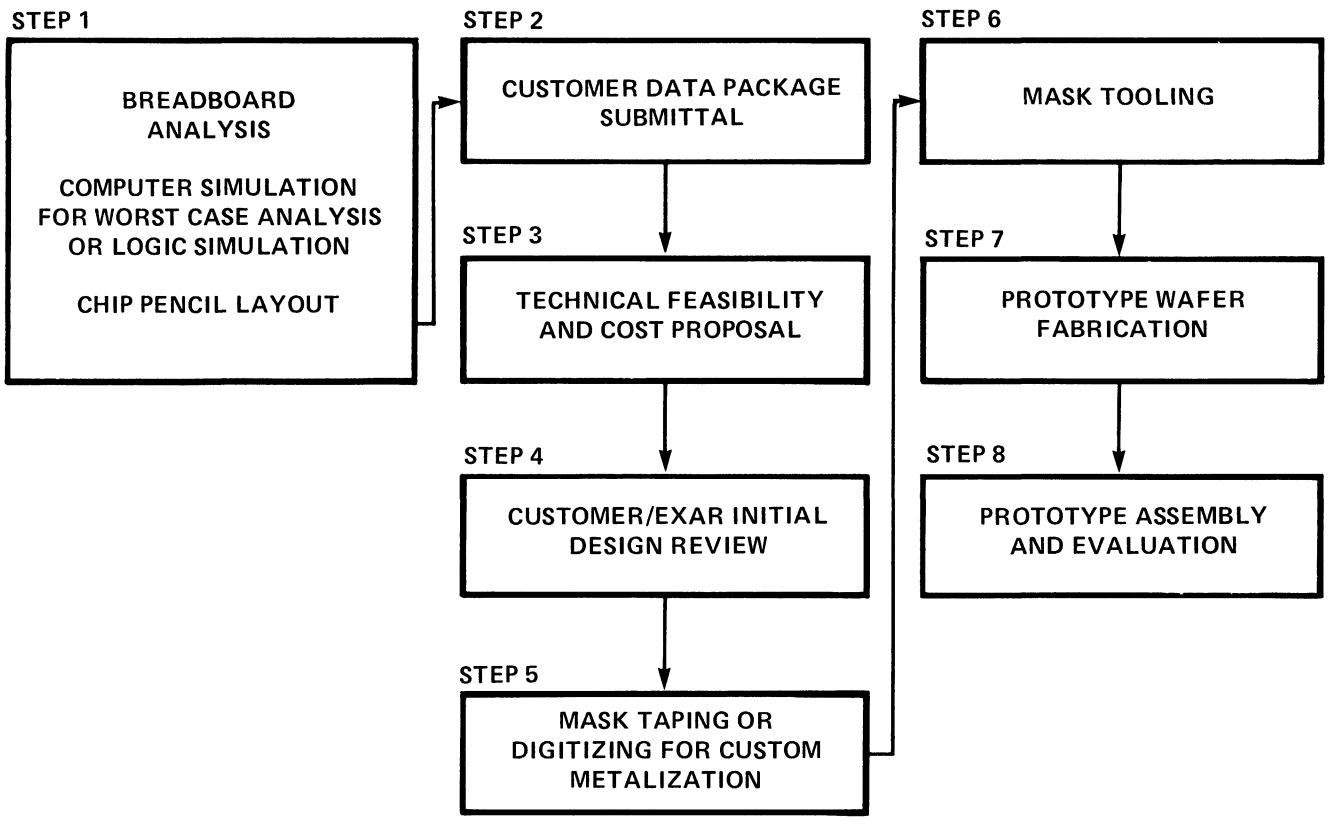
CAN EXAR SUPPLY CHIPS?

All of Exar's semi-custom products can also be supplied in chip form, for hybrid assemblies. Page 37 gives a detailed description of the electrical specifications, visual inspection criteria and the handling of shipping options available for monolithic chips.

CAN EXAR DO ENVIRONMENTAL SCREENING?

Exar has complete burn-in, environmental test and screening services available for temperature-stressing, thermal-shock or humidity and hermeticity tests. For a detailed analysis of your needs consult Exar's Marketing Department.

FLOW CHART OF TYPICAL SEMI-CUSTOM DEVELOPMENT



Economics of Semi-Custom Design

In developing either linear or digital custom circuits, one is always confronted with the following key question: for a given product type and production requirement, is it cheaper to develop a semi-custom or a full custom IC? Since the functional requirements of each custom IC program vary greatly, there is no general answer to the above question. However, based on Exar's long experience in both full and semi-custom IC design, and depending on the overall production requirements, it is possible to establish some sound economic guidelines for choosing the most cost-effective approach.

COST FACTORS INVOLVED

Any custom IC development, whether full or semi-custom, involves similar types of cost factors. These are:

1. Non-recurring engineering (NRE) or development costs.
2. Cost or unit price of the product in production quantities.

In the case of monolithic IC's, particularly for those which have relatively limited production volume, the development costs may be a significant factor in the cost of the end product. Therefore, when discussing the economics of custom IC's for medium to low production quantities, it is best to consider the cost trade-offs in terms of the "amortized unit price" of the IC at a given production volume. This amortized unit price is defined as the actual cost of each unit *including* its share of the development cost. As an example, a full custom IC may cost $50,000 to develop, and may be priced at $2.90 each at a 50,000 piece total production level. Then, its true amortized unit price including development costs will be $2.90 plus $1.00, or $3.90. Similarly, an equivalent semi-custom IC may cost $5,000 to develop and be priced at $3.20 each, at the same 50,000 production level. Then, its amortized per unit price will be $3.30, or approximately 20% cheaper than a full custom.

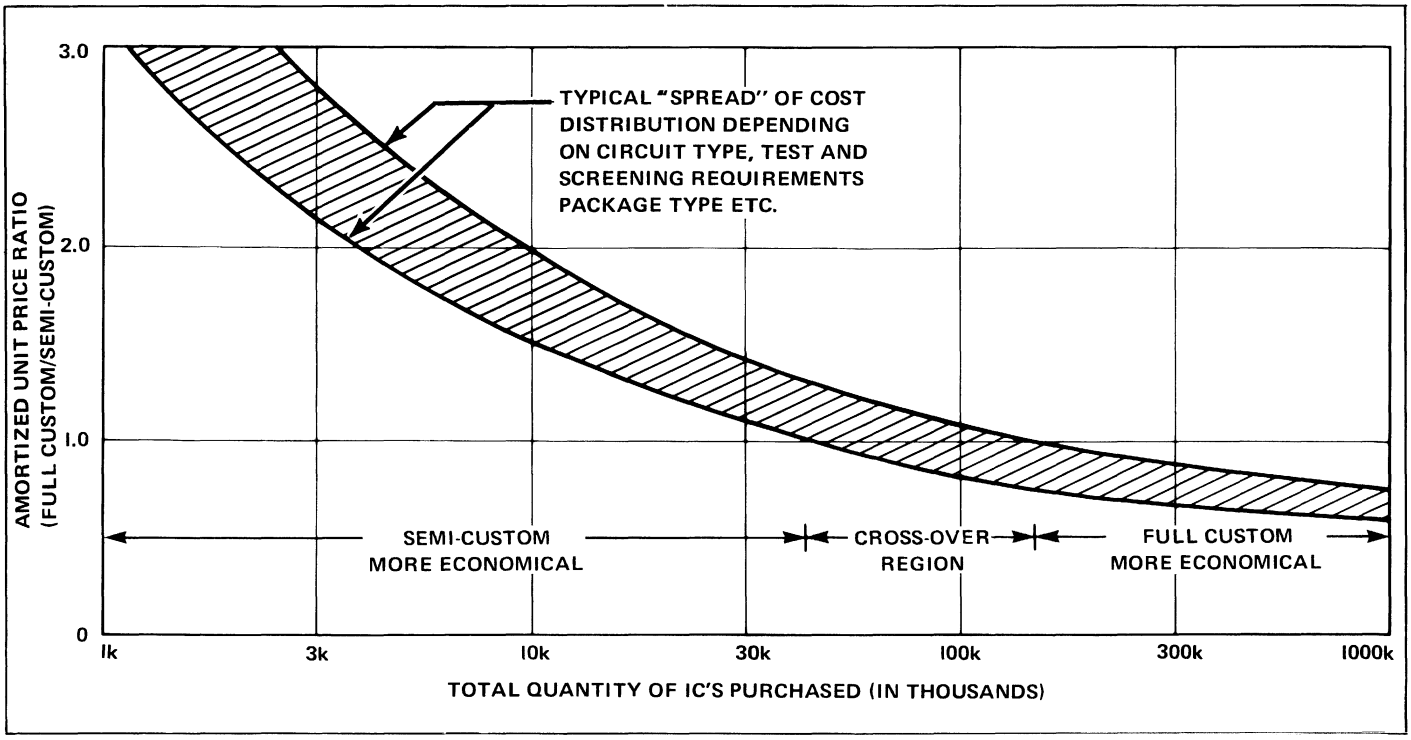
The figure below gives a comparative graph of the amortized unit price for a typical full custom design along with its equivalent in semi-custom form, for various production quantities. For comparison purposes, the relative "ratio" of the amortized unit price is plotted along the vertical axis. If this ratio is greater than 1.0, then the semi-custom method is the more cost-effective solution.

NO TWO IC'S ARE THE SAME

By definition, each custom IC type is unique: it has a special performance, interface or test requirement. Therefore, the cost comparison curve given below is shown as a "spread" rather than a single line. This is because, in addition to the production quantity, the cost of monolithic IC's also depends on the circuit complexity (i.e., yield), special test requirements and the IC package type.

The key information contained in the relative cost vs. quantity figure can be summarized as follows:

1. For total production requirements of 50,000 pieces or less, the semi-custom approach is definitely the most economical.
2. For production requirements of 200,000 pieces or more, the full custom design is more cost effective.
3. For production quantity requirements in the 50,000 to 200,000 pieces, the crossover point for the most economical approach depends strongly on the specifics of a particular IC function i.e., its special test, environmental screening and package requirements.



Typical Cost vs. Quantity Comparison of Full Custom and Semi-Custom Designs

Converting Semi-Custom to Full Custom

Exar is the only company that can offer you the advantages of semi-custom and full custom bipolar design programs because of our in-house complete semiconductor manufacturing capability. This unique capability gives us the ability to start a custom development program using a combination of our semi-custom Master Chips during the initial or early phases of a customer's product, taking full advantage of the low tooling cost and short development cycle. As a customer's product matures and its market expands, resulting in higher volume production run rates, Exar can convert the multiple semi-custom chip approach into a single custom IC, achieving a cost reduction and in many cases a performance improvement. The significant advantage of this type of program is that the risk associated with a custom development is greatly reduced; the IC design approach has been proven, production "bugs" are out of your product and your production line continues to flow during the full custom chip development. Once the custom chip is completely characterized and found acceptable, the semi-custom IC system in your product can be phased-out while the full custom IC is being phased-in.

SEMI- AND FULL CUSTOM COMBINATION –THE TWO-STEP DEVELOPMENT–

In many custom development programs one is faced with very short development times, and a rapid transfer into high volume production. Such a requirement does not leave room for lengthy development and design change or iteration cycles associated with conventional full custom IC design.

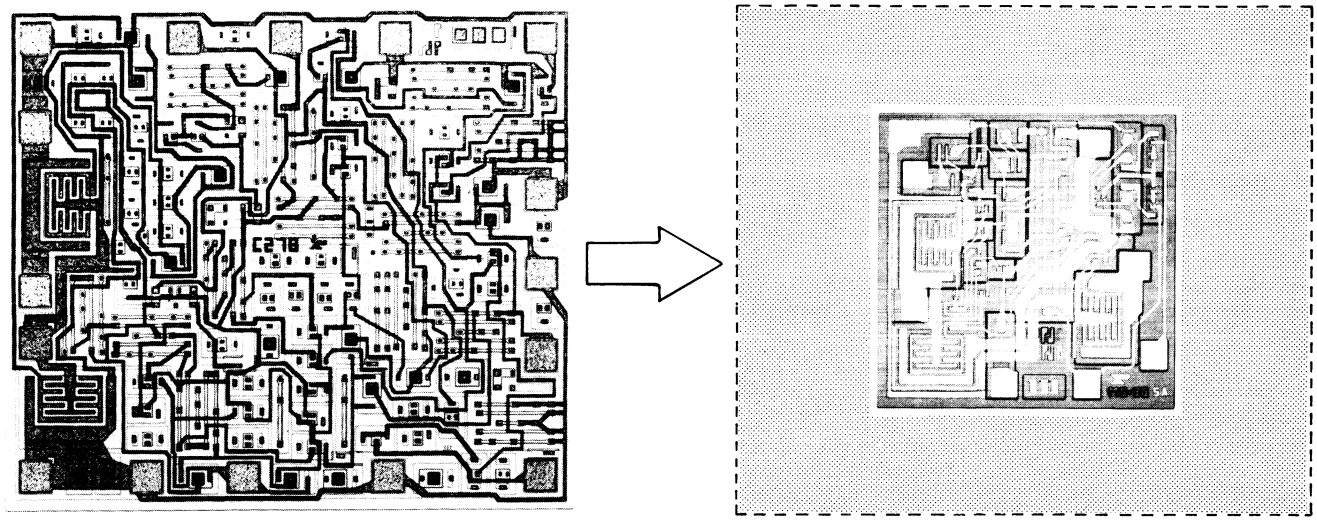
Exar's unusual capability of combining both full and semi-custom design capabilities and a complete wafer fabrication capability under one roof provides a unique solution to this problem: by initially developing the prototypes in a semi-custom form, and then converting them to full custom. In this manner, the customer has the "best of two worlds" in utilizing the conbination of these two technologies: the quick turn-around advantages of semi-custom Master Chips provide prototypes and the initial production units; the subsequent full custom design provides cost savings at high volume production. Yet, during this transistion, the customer is assured of a continous flow of product through its production line.

In such a *Two-Step* development, the semi-custom prototypes often serve as a "monolithic breadboard" to optimize and de-bug the final design. The performance of the semi-custom chip accurately simulates the characteristics of the final, full custom design. Yet, it allows one to perform design iterations or changes in a very efficient and cost-effective form. In fact, the only difference between the semi-custom and the full custom chip is the actual "size" of the silicon chip.

Once the design is satisfactory, conversion of a semi-custom to a full custom chip is very straight forward and relatively risk free: we simply remove the unused electrical components from the chip to reduce the chip size and pass the resulting cost savings to you in the form of reduced unit price.

The *Two-Step* development capability, i.e., start as semi-custom and finish as full custom, is a very powerful design technique. It avoids the risks associated with a conventional "black box" type custom design where one doesn't know, until the very last day of development, whether the circuit works or if it is manufacturable.

Since it avoids costly design iteration or modification cycles, the *Two-Step* program does *not* take any longer or cost more than the conventional full custom development; yet it gives one a very high degree of assurance that the final full custom unit will "work the first time".



Semi-Custom Design and Its Full Custom Equivalent

Full Custom Development

Exar offers a complete design and production capability for full-custom IC development using Exar's bipolar and I^2L technologies. This provides an excellent complement to Exar's unique semi-custom capability.

Exar's full-custom IC development and production capabilities offer complete flexibility to meet changing customer needs or design problems. We can develop a complete custom IC starting from your "black-box" specifications or reduce your working breadboard prototype to a monolithic chip. Alternately, if you have the facilities and resources to do the IC design and the layout, Exar will provide you with the device characteristics and IC layout rules for the particular process suitable to your design and review your IC layout for you. Then, Exar can generate the IC tooling and fabricate your IC prototypes for you.

YOUR FIRST STEP FOR FULL CUSTOM DESIGN

The following technical data package is required in order for Exar to provide you with a firm quotation for your full-custom development program:

1. Circuit block diagram with sub-blocks.
2. Circuit Schematic or Logic Diagram.
3. Description of circuit operation and pertinent application information.
4. Preliminary or objective device specification indicating min/max conditions and limits for the critical parameters (i.e., input/output voltage and current levels, operating frequency, timing diagrams, input/output impedances, power dissipation, etc.)
5. Production requirements and the desired development time table.

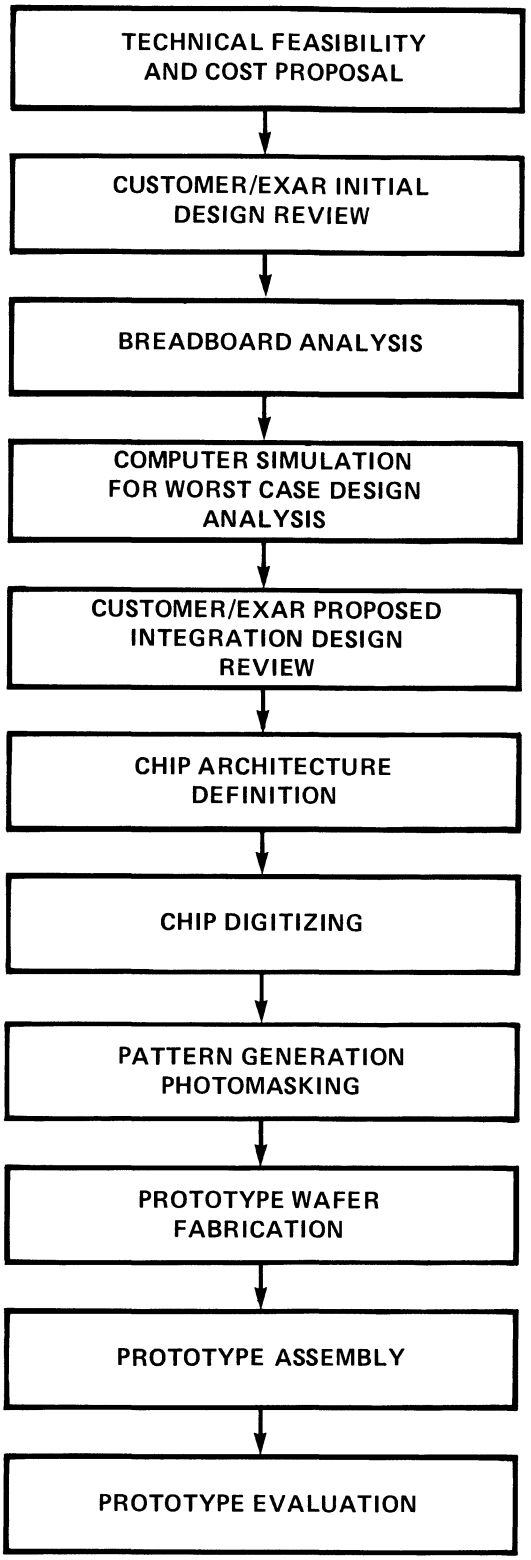
IC FABRICATION FROM CUSTOMER'S TOOLING

Exar has a complete in-house silicon wafer fabrication and processing line at its main manufacturing plant, in Sunnyvale, California. This facility is geared to handle 3-inch silicon bipolar or I^2L wafers, and is available for manufacturing custom IC's directly from a set of customer supplied IC tooling, in coordination with Exar's mask design department.

If you have a set of IC tooling (i.e., masks and composite overlays) or are contemplating having one designed for you, Exar's technical staff will be glad to review it for you to assure compatibility with Exar's technology and layout tolerances. Our wafer processing technology and capabilities are compatible with the industry standards, and with the technologies of other leading bipolar IC manufacturers.

For additional information on Exar's wafer fabrication services, contact Exar directly. We pride ourselves in our flexibility and quick response to your needs.

FLOW-CHART OF TYPICAL FULL CUSTOM DEVELOPMENT PROGRAM



Testing of Semi-Custom IC's

All production units of semi-custom IC's are 100% electrically tested and screened, to mutually agreed test specifications, using one of Exar's several computerized test systems. In addition, Exar's Quality Assurance Department performs an independent set of electrical tests on randomly selected samples of production units, prior to shipment, to assure conformity with Exar's Acceptable Quality Level (AQL) standards.

EXAR'S TEST CAPABILITIES

Exar can perform two basic types of tests for production IC's: (1) parametric testing which measures a specific parameter value (normally current or voltage) and compares it against pre-established limits; (2) functional testing which applies a series of operating conditions and compares the circuit under test with a known good device. These two types of tests can be performed both as steady state (DC) or dynamic (AC) measurements. Although DC tests are easily implemented by automated testers, AC tests are usually difficult and expensive to perform in production.

Exar has a complete computer-controlled IC test facility, to provide 100% electrical testing of IC chips either in wafer form, using automated wafer-probe stations, or in dual-in-line package form, using automatic handlers. Exar's test facility has four independent computer controlled test systems.

- **Fairchild 5000C Tester**

This is a fully automatic test system which can perform both functional and parametric DC tests, with an accuracy of 0.1%, at a rate of approximately 10 milliseconds per test. It can be used for AC tests, with additional interface circuits. It can handle four separate test stations simultaneously.

- **Fairchild Sentry 200 Tester**

This is an automated high-speed test system primarily intended for complex digital circuits. It can perform both DC and functional tests on logic or memory systems up to 48-pins. It operates four separate test stations from a central computer.

- **Teradyne J273 Tester**

This is a fully automated test system for AC and DC testing of linear circuits. It is designed for high-volume production testing, and operates four separate test stations simultaneously.

- **Logical/Servant-8 Tester**

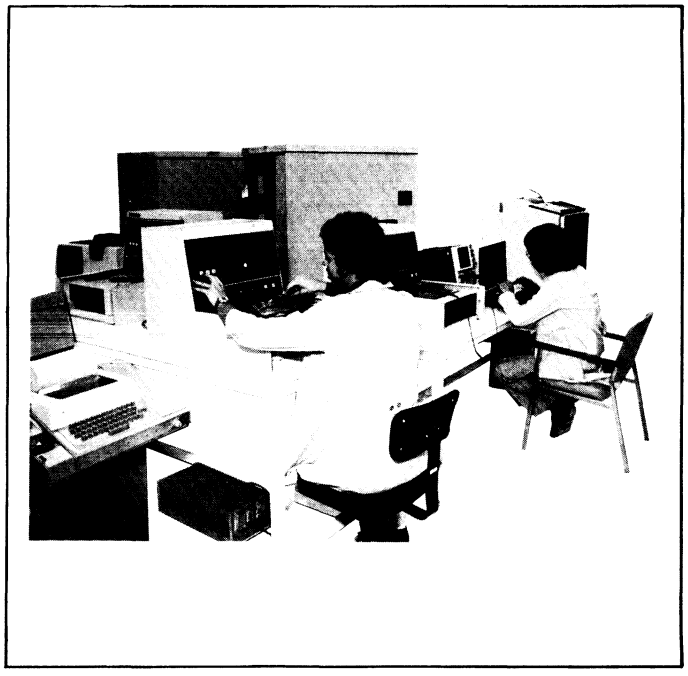
This is a computer-controlled tester especially designed for testing of digital semi-custom chips. It performs functional tests on complex logic arrays, up to 40-pin complexity.

Testing is one of the most critical steps in IC production. Therefore, to insure efficient and cost-effective testing of production IC's, it is essential that a preliminary *test plan* be prepared, jointly between customer and Exar, at an early stage of the prototype development effort. This preliminary test plan then leads to the final detailed test specifications, once the development prototypes are fully evaluated and characterized, and the circuit is ready to release to production.

TEST INTERFACE DEVELOPMENT

Before releasing a semi-custom IC into production, it is necessary to develop a complete test interface (i.e., the necessary test program software and the interface hardware or fixtures) which will allow the monolithic chip to be 100% tested using Exar's computer-controlled testers. This development effort normally requires *four* to *six* weeks to complete. However, it can be initiated in parallel with the IC development if a test plan is completed and a production commitment is made at the start of the program. There is normally a non-recurring engineering charge associated with this test interface development. This charge varies depending on the device specifications, test complexities and the follow-on production requirements.

Fairchild 5000C Test System



Fairchild Sentry 200 Test System

Linear Semi-Custom Design

The linear semi-custom design program is based on Exar's family of bipolar Master Chips. As described earlier, these Master Chips are fabricated through all the necessary device fabrication steps, except for the final step of "metal interconnection". They are then "customized" to form a monolithic IC simply by the application of a "custom" interconnection pattern.

Exar offers a very wide selection of the bipolar Master Chips. These chips vary in their voltage and current ratings, device characteristics and types, as well as in the number of components available on each chip.

AVAILABLE MASTER CHIPS

Exar currently has five different bipolar Master Chips in production, with additional chips in development for future applications. Three of these chips, the XR-A100, XR-B100 and XR-F100 are all fabricated with the same manufacturing process and have a maximum operating voltage rating of 20 volts. The XR-C100 and the XR-D100 Master Chips are designed for 25 volt and 36 volt maximum operating voltages, respectively. A brief outline of the key features of these five bipolar Master Chips are given below:

- **Master Chip XR-A100**

This chip is rated for a maximum operating voltage of 20 volts. The chip size is 73x83 mils and contains 260 components, including two high-current (200mA) NPN transistors for such applications as audio output stages, relay-drivers or high current voltage regulators. It can accommodate up to 16 pins, and is a direct replacement for Monochip A. A detailed description of the XR-A100 chip is given on page 11.

- **Master Chip XR-B100**

This chip is rated for a maximum operating voltage of 20 volts. Its size is 85x85 mils and contains 300 passive and active components, and is a direct replacement for Monochip B. It contains a large number (69) small signal NPN transistors for complex linear or linear and digital circuits. It can accommodate up to 24 pins. A more detailed description of this chip is given on page 12.

- **Master Chip XR-C100**

This is a 76x78 mil chip and is rated for 25 volt maximum operating voltage. It contains 201 active and passive components, including two 100-mA NPN transistors. It can accomodate up to 19 pins. See page 13 for chip layout and component description.

- **Master Chip XR-D100**

This is a high-voltage Master Chip, designed for 36 volt maximum operating voltage. Its dimensions are 80x81 mils. It contains 209 active and passive components and is a direct replacement for Monochip D. The XR-D100 contains dual-collector PNP transistors especially suited for current sources or active loads and can accommodate up to 16 pins. Chip layout and component locations are shown on page 14.

- **Master Chip XR-F100**

This is the largest linear Master Chip (98x115mils) and contains 460 components, including four 200-mA high current NPN transistors and a large number of dual-collector PNP transistors. It is a direct replacement for Monochip F and can accommodate up to 24 pins. The layout and component locations are shown on page 15.

COMPONENT UTILIZATION

How many of the components can you actually use on each chip? The answer to this question depends mainly on the character of your circuit. A linear design in which various circuit blocks follow each other (without a multitude of cross-connections) and where pins can be chosen freely is easy to interconnect: with such circuits, one can achieve a component utilization above 90%. If however, some of the pins are fixed, or there are a lot of cross-connections, the layout job becomes more difficult and you may only be able to use 70% of the components.

The bipolar Master Chips are laid out to provide easy routing of metal interconnection paths on the chip. In addition, a multiplicity of low-resistance cross-unders are provided on the chip to simplify the interconnection layout. Based on our experience in the layout of various Master Chips, the following component utilization table provides a rough guideline in estimating the layout efficiency of various bipolar Master Chips.

COMPONENT UTILIZATION GUIDE FOR LINEAR MASTER CHIPS

MASTER CHIP TYPE	EASY			SOMEWHAT DIFFICULT			DIFFICULT		
	NPN	PNP	RESISTANCE	NPN	PNP	RESISTANCE	NPN	PNP	RESISTANCE
XR-A100	40	12	120 k ohm	45	15	140 k ohm	48	16	160 k ohm
XR-B100	50	7	150 k ohm	52	9	170 k ohm	58	12	200 k ohm
XR-C100	35	6	80 k ohm	40	7	90 k ohm	45	8	120 k ohm
XR-D100	38	20*	90 k ohm	41	24*	100 k ohm	45	26*	120 k ohm
XR-F100	60	40*	250 k ohm	70	46*	300 k ohm	80	54*	340 k ohm

*Dual-collector PNP's are counted as two singles.

XR-A100 Master Chip

Chip Size: 73 x 83 mils

Total Components: 260

NPN Transistors

Small Signal: 58

High Current: 2

PNP Transistors: 18

Schottky Diodes: 15

Pinch Resistors

30 kΩ: 4

100 kΩ: 4

Bonding Pads: 16

Max. Operating Voltage:

20V

Diffused Resistors

200 Ω: 16

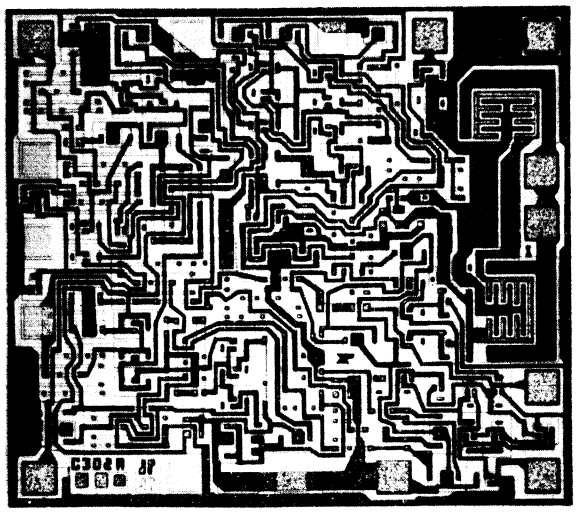
450 Ω: 43

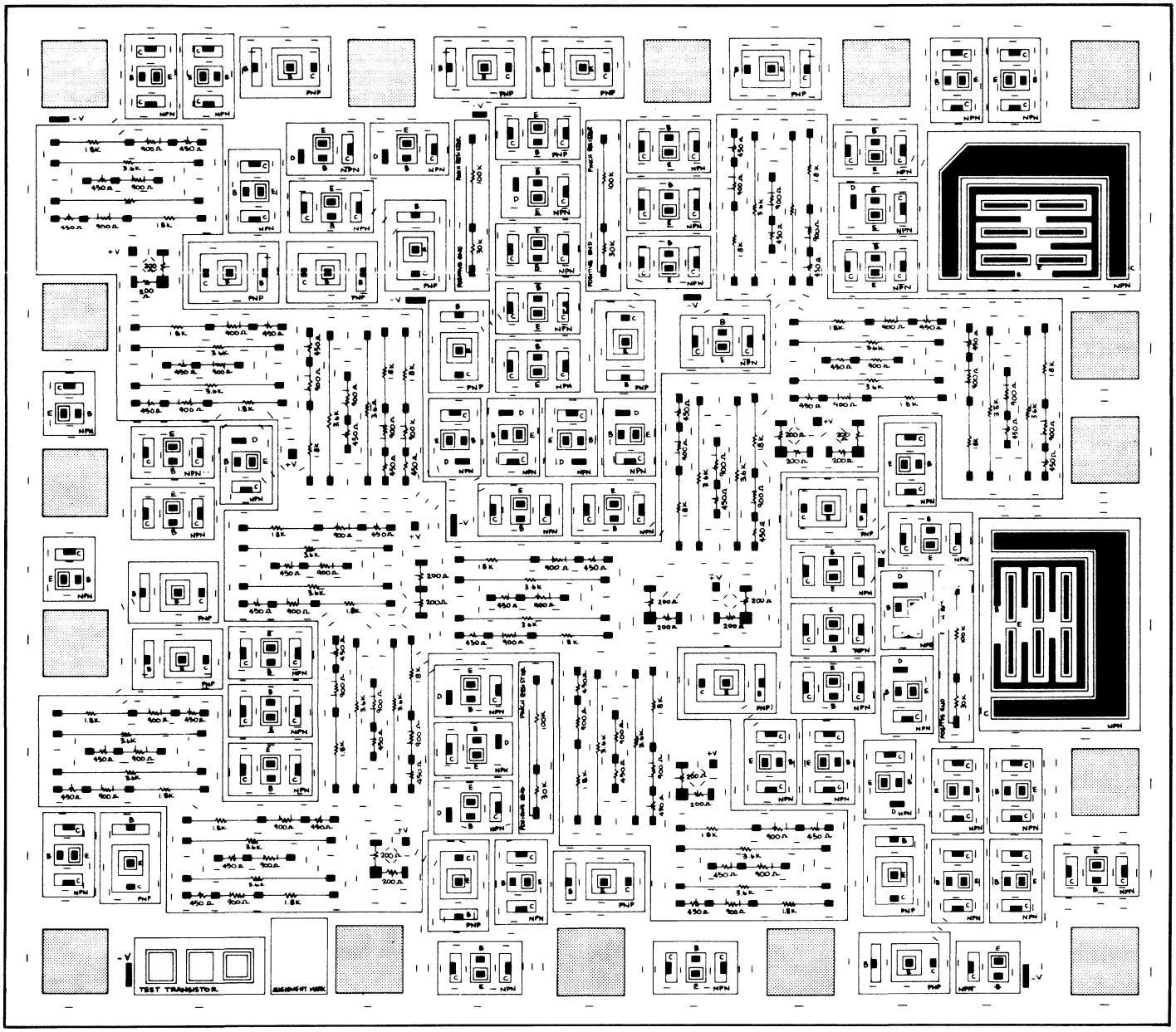
900 Ω: 43

1.8 kΩ: 29

3.6 kΩ: 28

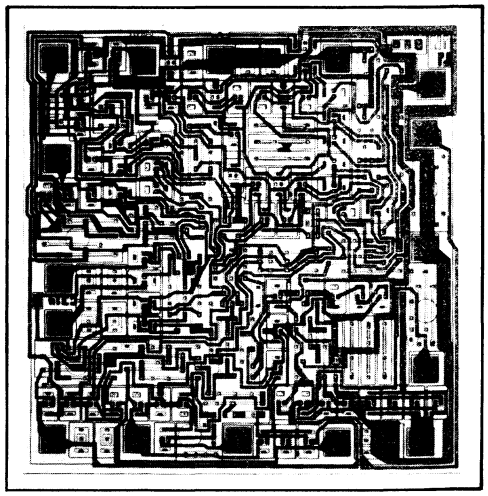
Total Resistance: 214 kΩ

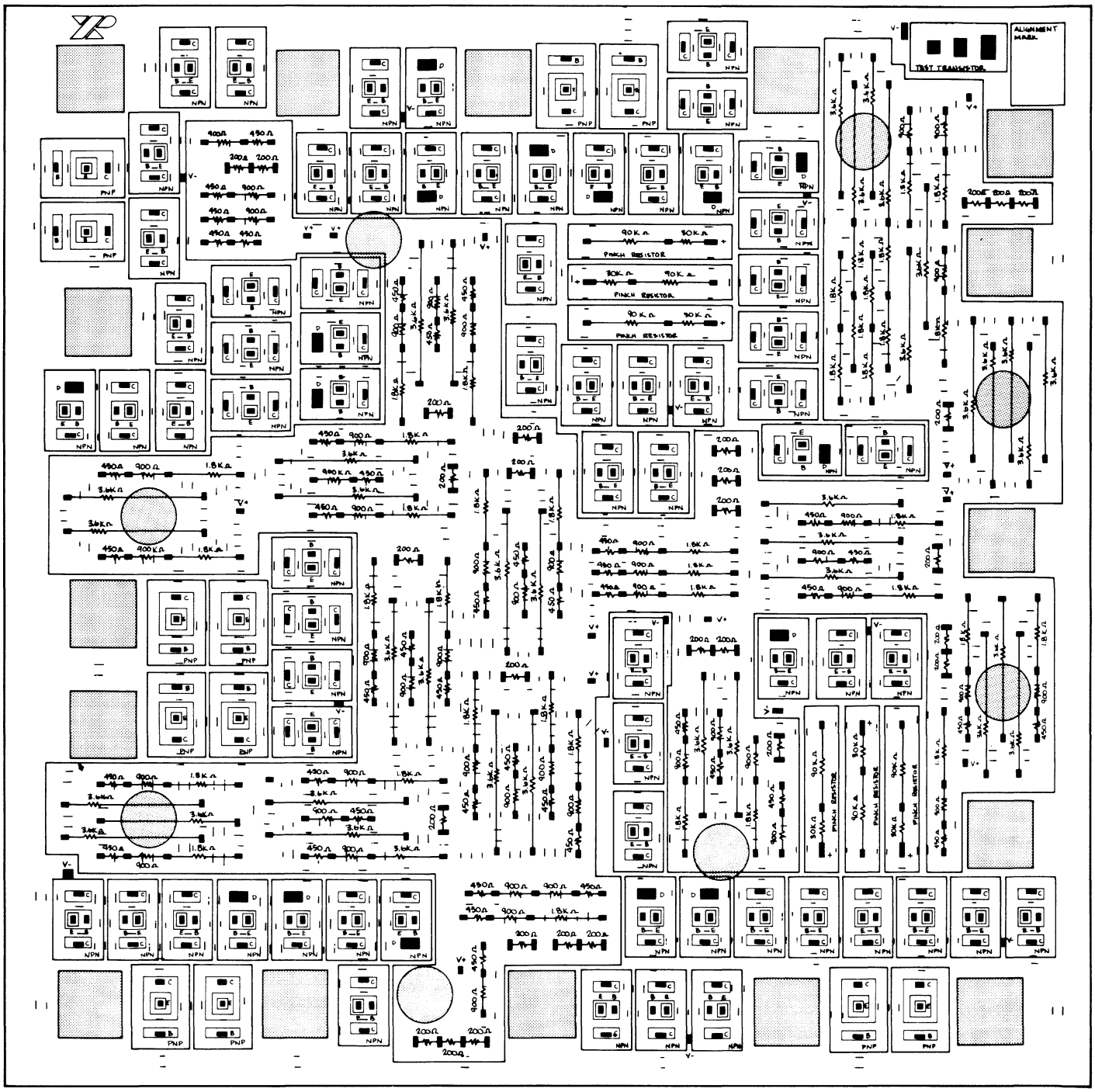




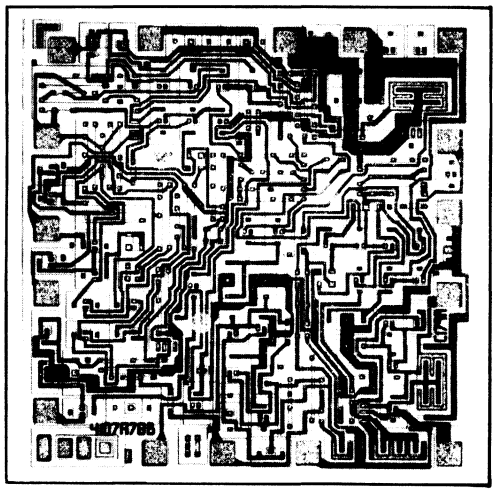
XR-B100 Master Chip

Chip Size: 85 x 85 mils
Total Components: 300
NPN Transistors
  Small Signal: 69
  High Current: None
PNP Transistors: 12
Schottky Diodes: 16
Pinch Resistors
  30 kΩ: 6
  100 kΩ: 6
Bonding Pads: 24
Max. Operating Voltage:
  20V
Diffused Resistors:
  200 Ω: 27
  450 Ω: 44
  900 Ω: 45
  1.8 kΩ: 39
  3.6 kΩ: 36
Total Resistance: 265 kΩ





XR-C100 Master Chip



Chip Size: 76 x 78 mils
Total Components: 201
NPN Transistors
- Small Signal: 49
- Common Collector: 8
- High Current: 2

PNP Transistors
- Lateral PNP: 8
- Substrate PNP: 2

Schottky Diodes: 3
Pinch Resistors
- 30 kΩ: 5
- 100 kΩ: 1

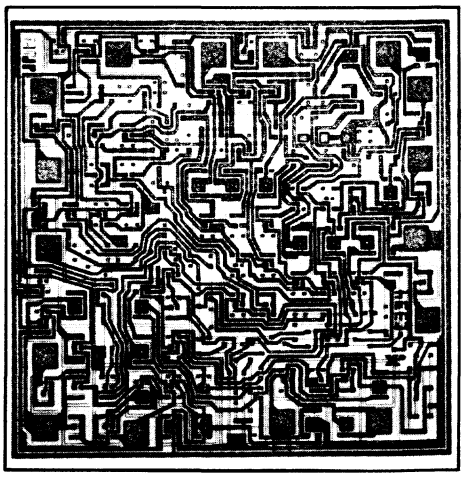
Bonding Pads: 19
Max. Operating Voltage: 25V
Diffused Resistors
- 59 Ω: 4
- 100 Ω: 4
- 150 Ω: 10
- 200 Ω: 10
- 400 Ω: 30
- 800 Ω: 29
- 1.6 kΩ: 20
- 3.2 kΩ: 15
- 5 kΩ: 4

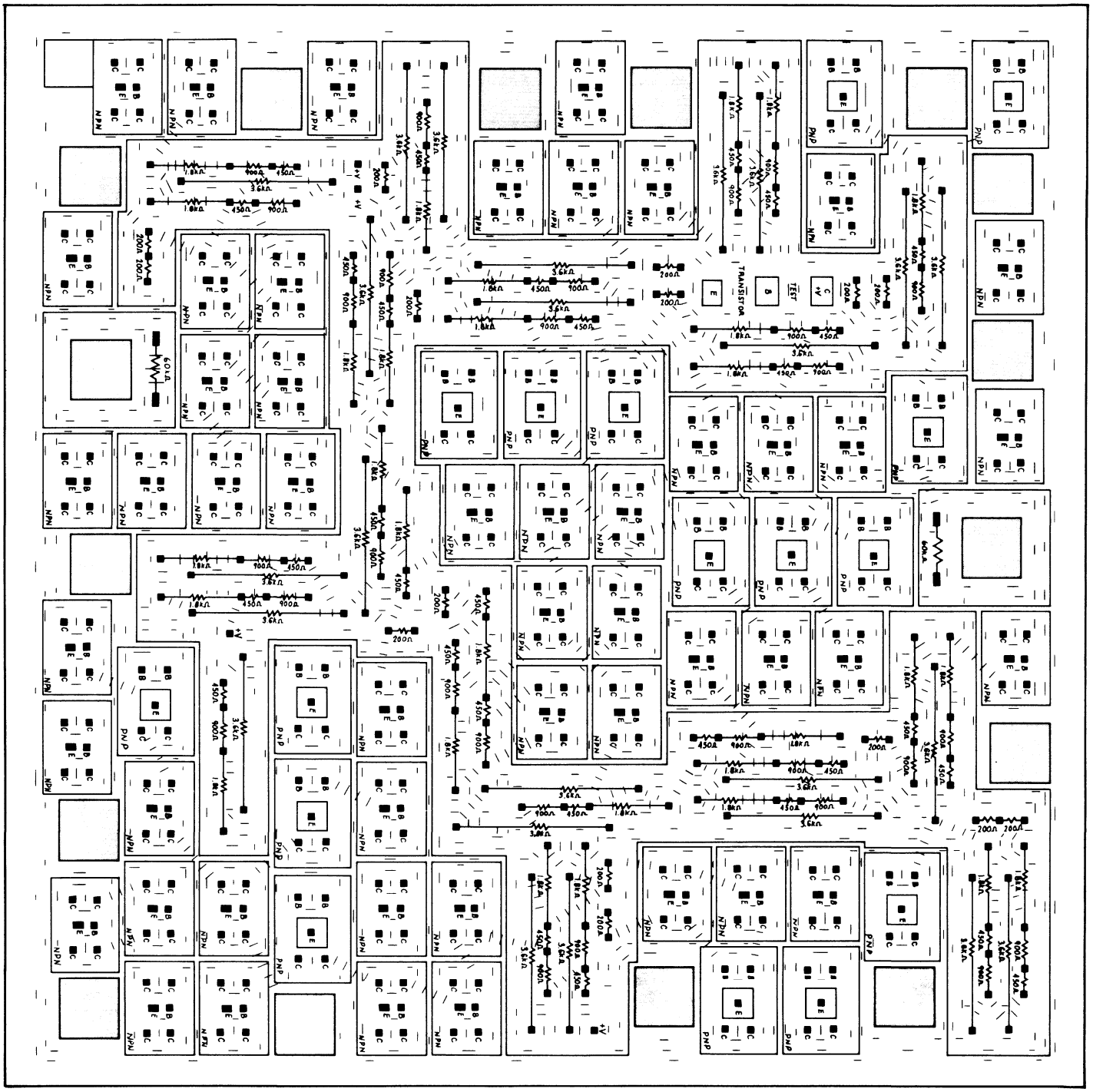
Total Resistance: 140 kΩ

XR-D100 Master Chip

Chip Size: 80 x 81 mils
Total Components: 209
NPN Transistors
  Small Signal: 50
  High Current: None
Dual PNP Transistors: 16
Schottky Diodes: None
Pinch Resistors
  60 kΩ: 2

Bonding Pads: 16
Max. Operating Boltage: 36V
Diffused Resistors
  200 Ω: 15
  450 Ω: 29
  900 Ω: 28
  1.8 kΩ: 29
  3.6 kΩ: 24
Total Resistance: 180 kΩ



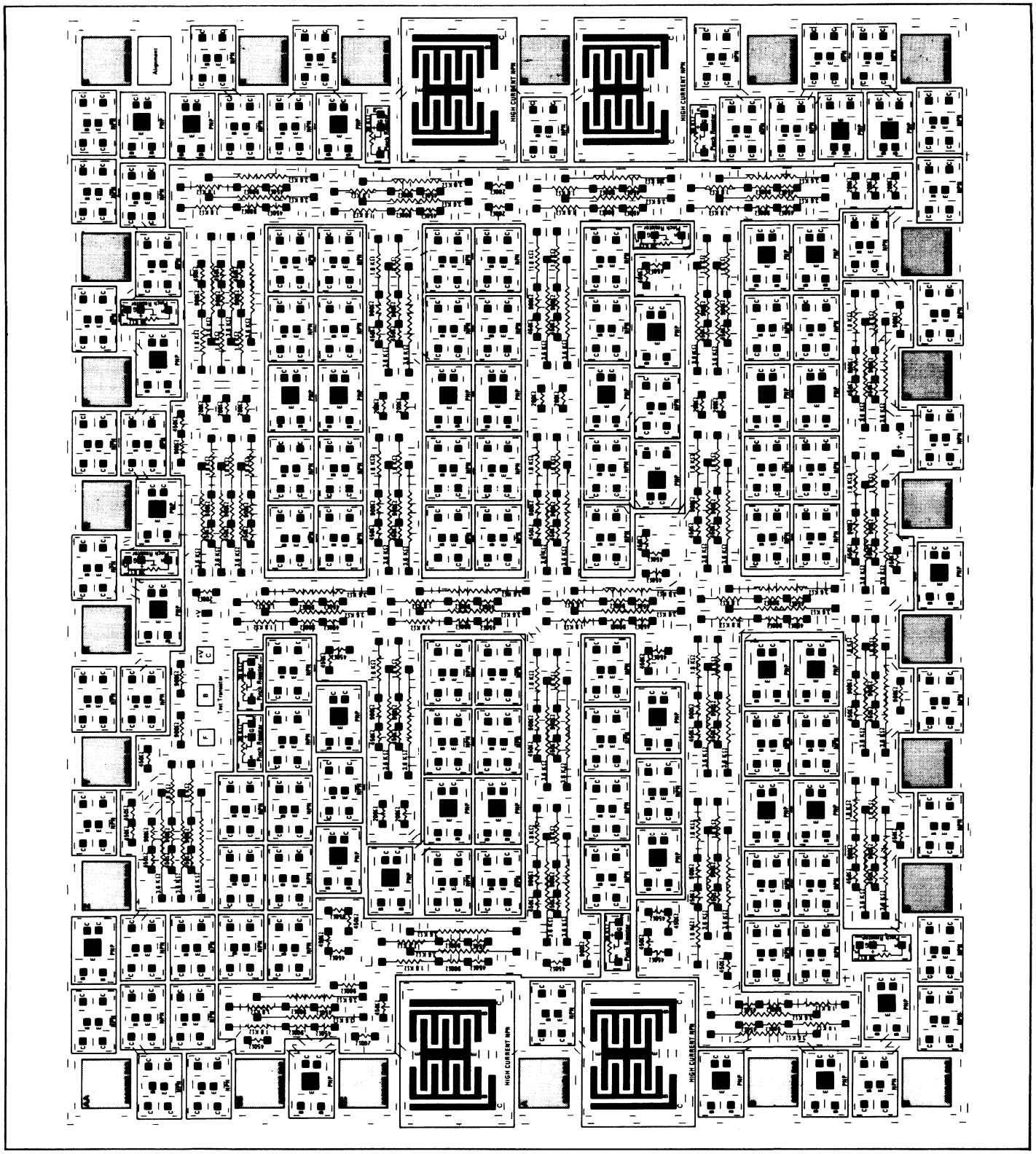


XR-F100 Master Chip

Chip Size: 98 x 115 mils
Total Components: 472
Bonding Pads: 24
Maximum Operating Voltage:
20 V

NPN Transistors
Small Signal: 93
High Current: 4
Dual PNP Transistors: 36
Total Resistance: 425 kΩ
Pinch Resistors: 9 30 kΩ

Diffused Resistors
200 Ω: 18
450 Ω: 90
900 Ω: 68
1.8 kΩ: 61
3.6 kΩ: 61



Linear Semi-Custom Design Cycle —Six Simple Steps—

The basic linear semicustom design program involves only *6 simple steps,* from the beginning of circuit design to completion of monolithic prototypes. The first three of these steps are done by the customer in consultation with Exar; the last three are preformed by Exar:

Step 1

Customer designs and breadboards his circuit using Linear Design Kit.

Customer purchases Exar's Linear IC Design Kit, made up of a comprehensive Design Manual and 34 monolithic kit parts or building blocks. Customer then breadboards his circuit and evaluates its performance using these kit parts. The electrical characteristics of kit parts are virtually identical to those which will be on the finished IC chip. Thus, this step provides a true breadboard simulation of final IC performance.

Step 2

Customer does circuit layout.

After completion of breadboard evaluation, customer prepares a layout of the circuit on the selected Master Chip by following the basic layout rules given in the Design Manual. The layout is done simply by interconnecting appropriate device terminals with pen or pencil lines on oversize drawings of the Master Chips supplied with the kit.
NOTE: As an option, Exar also offers a layout service, at a nominal charge.

Step 3

Customer submits layout to Exar for review:

Exar reviews the circuit layout and schematic to check the following:

a) That basic circuit function is feasible
b) No layout rules are violated
c) Circuit layout accurately represents the circuit schematic.

NOTE: Steps 1, 2, and 3 are done at ***no cost*** *to the customer, except for the nominal cost of the Linear Design Kit. Exar offers free consulting service and design advice during these first three steps. The "formal" part of the program is initiated at the completion of Step 3.*

Step 4

Exar generates custom interconnection pattern.

Using Master Chip circuit layout supplied by the customer, Exar generates a custom interconnection pattern, or "metal mask" to be applied to pre-fabricated Master Chip wafers.

Step 5

Exar fabricates customized IC wafers.

Exar applies the custom interconnection patterns to pre-fabricated Master Chip wafers. These wafers are then tested for semiconductor device characteristics (such as resistor values, diode and transistor characteristics) using special "test-patterns" etched on the wafer. The wafers are then accepted as "qualified wafer" if these device parameters are within the specified limits (see Table of Electrical Characteristics listed on pages 20 and 21).

Step 6

Exar assembles and delivers monolithic prototypes.

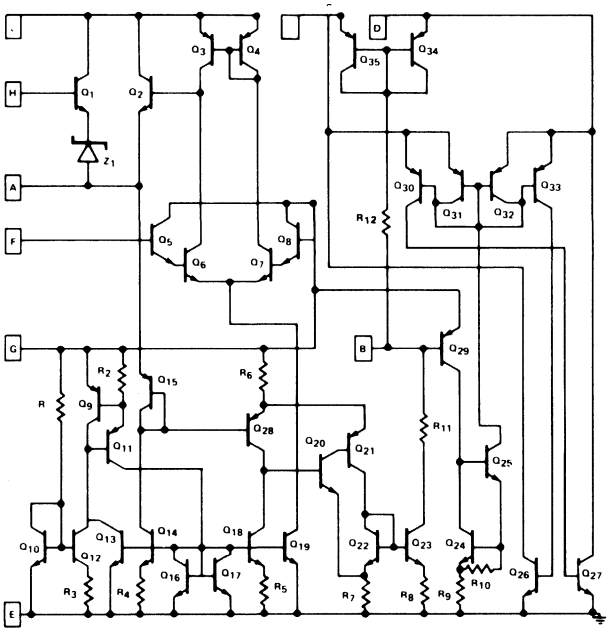
The customized IC wafers are scribed or cut into individual IC chips. After a visual inspection, a number of these custom IC chips are assembled in dual-in-line IC packages and delivered to the customer for electrical evaluation, to conclude the program.

In addition to the monolithic prototype IC's, the following technical information is also delivered to the customer:

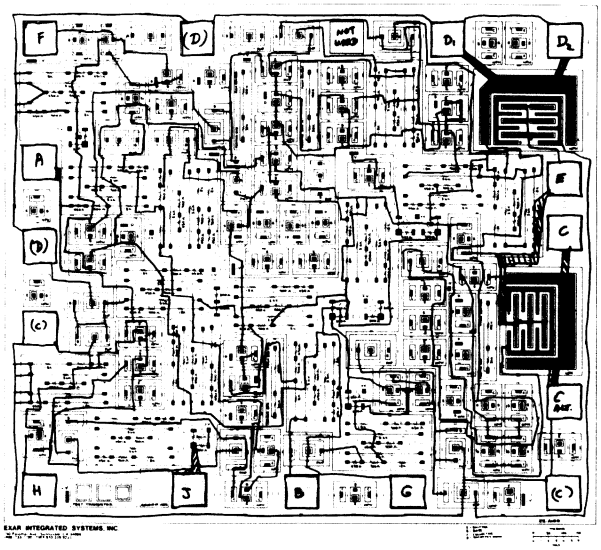
a) A printout of device characteristics measured in Step 5, using special "test-patterns" on the IC wafers.
b) An enlarged photo-micrograph of the finished IC chip showing the custom interconnection pattern.

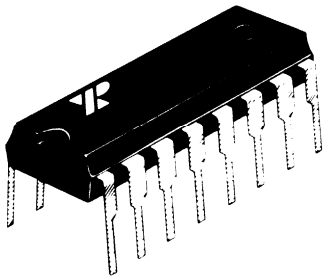
The above information verifies the quality of the IC devices and the accuracy of the custom interconnection patterns applied to the Master Chip wafer.

CIRCUIT SCHEMATIC

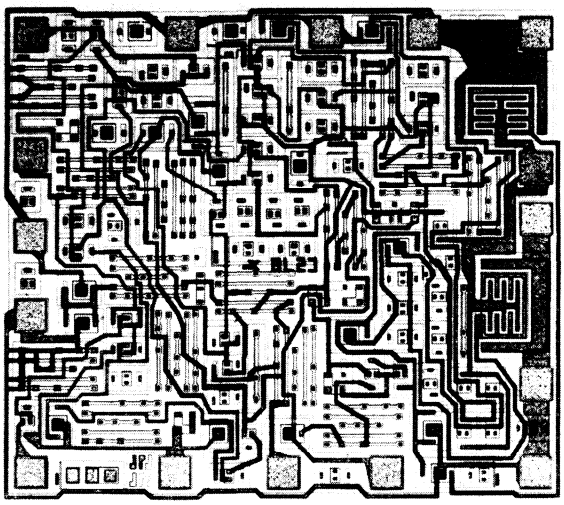


PENCIL LAYOUT

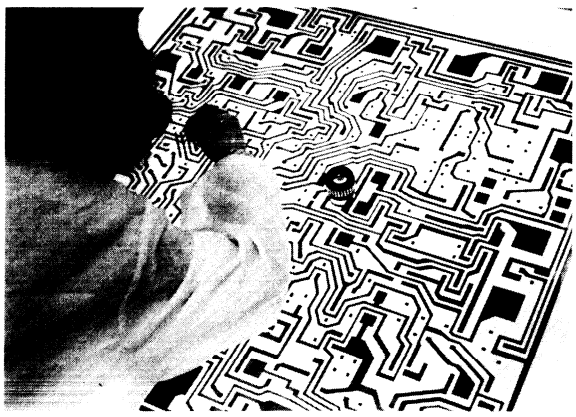




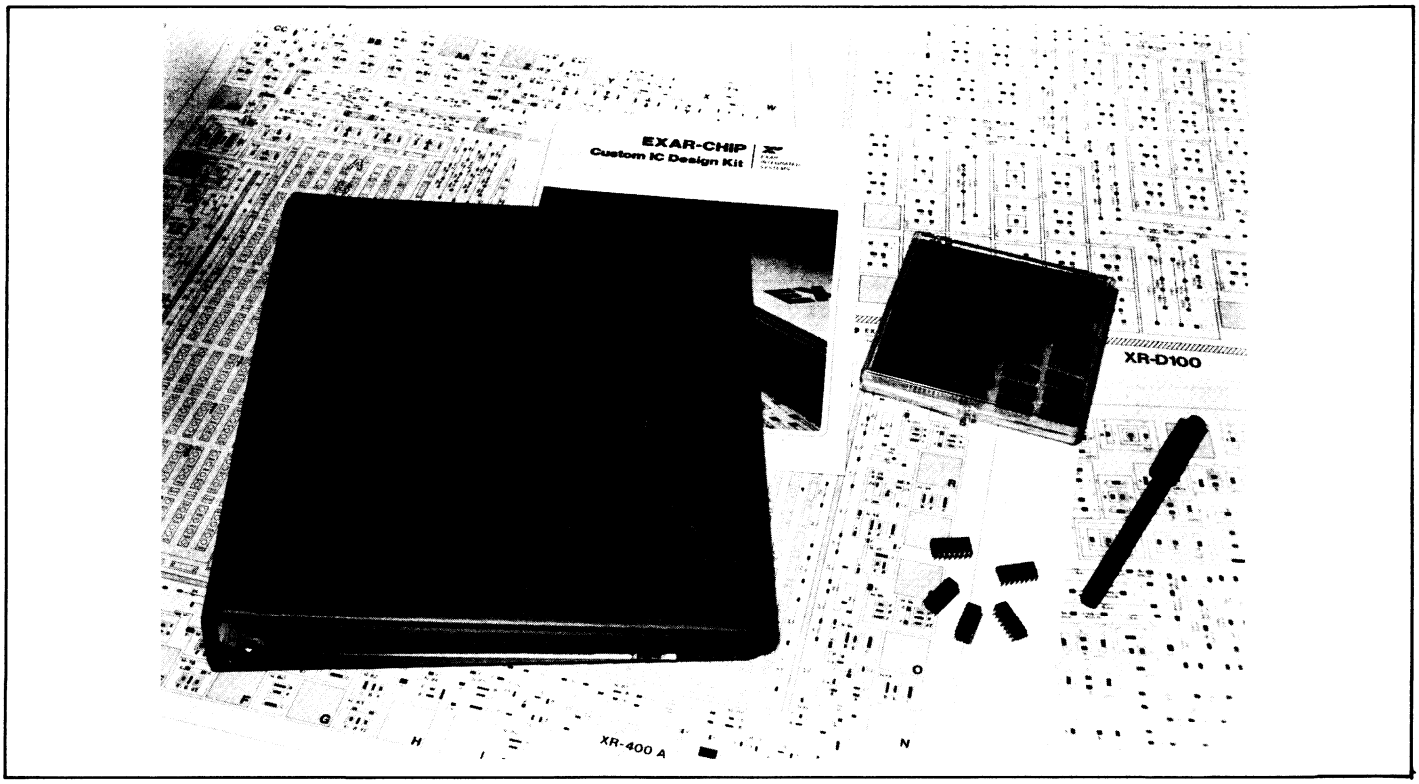
FINISHED SEMI-CUSTOM CHIP



MASK PREPARATION



Linear Design Kit



Exar's Linear Design Kit is comprised of thirty-four monolithic "kit parts" or breadboard components, a comprehensive Linear Design Manual, and a number of layout forms corresponding to Exar's Linear Master Chips. This Design Kit provides an ideal vehicle for the customer to do his own semi-custom IC design: he can evaluate his breadboard performance using the kit parts, and then proceed to do his own layout on the Master Chip work sheet.

The Linear Design Manual provided as a part of the Design Kit gives a detailed description of the basic guidelines and rules of IC design, evaluation, and layout. It also describes the electrical characteristics of each type of component available in the Master Chips, and gives some of the anticipated parameter distribution and "worst-case" tolerances associated with each. In addition, several design and layout examples are provided, to demonstrate the efficient use of the IC chips.

Once the breadboard evaluation is complete, the designer is ready to start his own IC layout using the appropriate Master Chip layout form supplied with the kit. When this layout is ready, and is reviewed by Exar, the formal part of the semi-custom development is ready to start.

TECHNICAL ASSISTANCE

If any special or unusual circuit design or layout problems are encountered in the preparation of your semi-custom IC layout Exar's technical staff will be glad to review your design problem and provide technical guidance. In many cases, it is beneficial to call Exar for a preliminary discussion of your custom IC needs, even before you decide to buy a Design Kit.

ADDITIONAL KIT PARTS

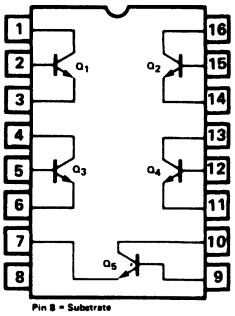
The amount of kit parts supplied as a part of the Linear Design Kit are sufficient for most designs. However, if additional kit parts are required to complete your evaluation, these can be obtained either directly from Exar, or through your local Exar technical representative.

CONTENTS OF LINEAR DESIGN KIT

PART NO.	DESCRIPTION	NO. OF ARRAYS IN KIT	DEVICES PER ARRAY	APPLICABLE MASTER CHIP
XR-B101	Small Signal NPN Transistor Array (20 Volt Process)	8	5	All Except XR-D100
XR-D101	Small Signal NPN Transistor Array (36 Volt Process)	8	5	XR-D100 only
XR-B102	Lateral PNP Transistor Array (20 Volt Process)	4	5	All Except XR-D100
XR-D102	Dual Collector Lateral PNP Array (36 Volt Process)	4	4	XR-D100 and F100
XR-A103	Schottky-Clamped NPN's and High-Current NPN's	4	5	All Except XR-D100
XR-A104	Medium Value Diffused Resistor Array	4	9	All Master Chips
XR-A105	High and Low Value Resistor Array	2	9	All Master Chips
	Total Arrays	34		
	Linear Design Manual	1		All Master Chips

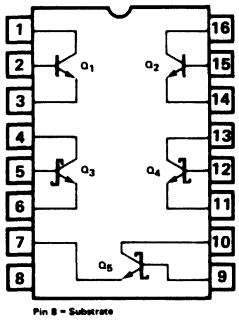
Components in Linear Design Kit

XR-B101 AND XR-D101 MONOLITHIC SMALL-SIGNAL NPN TRANSISTOR ARRAYS



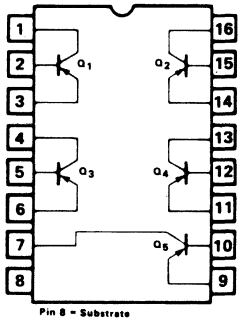
Each package contains five identical small signal NPN transistors. XR-B101 transistors correspond to NPN transistors available on XR-A100, XR-B100, XR-C100 and XR-F100 Master Chips. XR-D101 transistors are available only on XR-D100 chip.

XR-A103 SPECIAL PURPOSE NPN TRANSISTORS



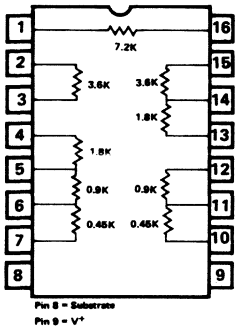
The XR-A103 contains two high-current (200 mA) NPN transistors (Q_1 and Q_2); and three Schottky-clamped small-signal NPN transistors (Q_3, Q_4 and Q_5). The high-current transistors are available only on XR-A100, XR-C100 and XR-F100 chips. The Schottky-clamped transistors are available on XR-A100 and XR-B100.

XR-B102 MONOLITHIC LATERAL PNP TRANSISTOR ARRAY



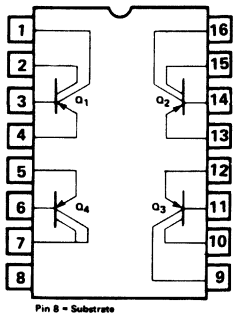
The XR-B102 chip contains five identical lateral PNP transistors. These are available on all chips except XR-D100.

XR-A104 DIFFUSED RESISTOR ARRAY



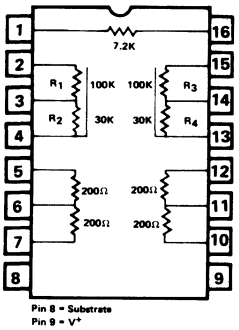
The XR-A104 chip contains an array of monolithic diffused resistors. Note that pins 8 and 9 of the package must be connected to the most negative and the positive voltages, respectively. The electrical characteristics of XR-A104 resistors are applicable to all bipolar Master Chips.

XR-D102 MONOLITHIC DUAL-COLLECTOR PNP TRANSISTOR ARRAY



XR-D101 contains four dual-collector lateral PNP transistors, which are available on the XR-D100 and the XR-F100 Master Chips. The collectors of Q_1, Q_2 and Q_3 are available separately; the two collectors of Q_4 are shorted together internally.

XR-A105 RESISTOR ARRAY



XR-A105 contains two sets of high-value "pinch-resistors" and two sets of low-value diffused resistors, and a 7.2 KΩ diffused resistor. Pins 4 and 13 indicate the positive terminals of the pinch-resistors. Pins 8 and 9 must be connected to the most negative and the positive voltages, respectively. The electrical characteristics of XR-A105 resistors are applicable to all bipolar Master Chips.

Electrical Characteristics of Linear Master Chip Components

The following tables list the electrical characteristics of the circuit components available on Exar's linear Master Chips. Whenever applicable, the "worst case" tolerances and the parameter distributions are also listed. The parameter distributions are given in terms of the standard deviation or the "sigma-limit."

1. Small-Signal NPN Transistors

PARAMETERS	TYPICAL VALUES	σ-LIMIT	WORST CASE TOLERANCE
Current gain (h_{FE}) @ 1 mA, 5V	180	–	80 – 300
Temperature Coefficiency of h_{FE}			
-55°C to 25°C	+0.5%/°C	–	–
25°C to 125°C	+1%/°C	–	–
Matching of h_{FE}	–	3%	10%
Breakdown voltage (LV_{CEO})			
A100/B100/F100 Chips	23V	–	20 – 30V
C100 Chip	27V	–	25 – 35V
D100 Chip	40V	–	36 – 50V
Collector-Base Leakage Current @ 20V	1 nA	–	0.1 – 50 nA
Cutoff Frequency (f_T) @ 5 mA	500 MHz	–	–
Storage Time (t_S)	50 nsec	–	–
Saturation Resistance (All except D100)			
One collector contact	100 Ohms	±50 Ohms	60 –160 Ohms
Two collector contacts	50 Ohms	±20 Ohms	30 – 80 Ohms
Saturation Resistance (D100 chip)			
One collector contact	300 Ohms	±100 Ohms	150 – 480 Ohms
Two collector contacts	150 Ohms	±50 Ohms	75 – 240 Ohms

2. High-Current NPN Transistors (A100/C100 and F100 Chips Only)

PARAMETERS	TYPICAL VALUES	σ-LIMIT	WORST CASE TOLERANCE
Current Gain (h_{FE})			
@ 1 mA, 5V	180	–	80 – 300
@ 100 mA, 5V	100	–	50 – 200
Temperature Coefficient of h_{FE}			
-55°C to 25°C	+0.5%/°C	–	–
25°C to 125°C	+1%/°C	–	–
Matching h_{FE}	–	3%	10%
Breakdown Voltage (LV_{CEO})			
XR-A100/XR-F100	23V	–	20 – 35V
XR-C100	27V	–	25 – 35V
Collector-Base Leakage Current @ 20V	20 nA	–	1 – 500 nA
Cutoff Frequency (f_T)	100 MHz	–	–
Storage Time (t_S)	200 nsec	–	–
Saturation Resistance	5 Ohms	±1 Ohm	3 – 8 Ohms

3. Lateral PNP Transistors

PARAMETERS	TYPICAL VALUES	σ-LIMIT	WORST CASE TOLERANCE
Current Gain (h_{FE}) @ 100 μA, 5V	20	–	5 – 80
Temperature Coefficient of h_{FE}	±0.1%/°C	–	–
Matching of h_{FE}	–	5%	15%
Breakdown Voltage (LV_{CEO})			
All except XR-D100	35V	–	25 – 40V
XR-D100	45V	–	36 – 60V
Collector-Base Leakage Current @ 20V	5 nA	–	0.1 to 100 nA
Cutoff Frequency (f_T)	5 MHz	–	–
Storage Time (t_S)	500 nsec	–	–
Saturation Resistance	600 Ohms	±100 Ohms	300 – 900 Ohms

4. Transistors Connected as Diodes (Collector and Base Shorted)

PARAMETERS	TYPICAL VALUES	σ-LIMIT	WORST CASE TOLERANCE
Small NPN			
Forward Voltage Drop @ 1 mA, 25°C	0.74V	±200 mV	0.68 – 0.8V
Forward Voltage Matching	–	2 mV	6 mV
Forward Voltage Tracking	–	5 μV/°C	15 μV/°C
Lateral PNP			
Forward Voltage Drop @ 200 μA, 25°C	0.70V	±200 mV	0.62 – 0.76V
Forward Voltage Matching	–	3 mV	6 mV
Forward Voltage Tracking	–	8 μV/°C	25 μV/°C

5. NPN Base-Emitter Junctions Used as Zener Diodes

PARAMETERS	TYPICAL VALUES	σ-LIMIT	WORST CASE TOLERANCE
Small NPN Transistors			
Breakdown Voltage @ 100 μA			
A100/B100/F100 chips	6.35V	±0.15V	5.9 – 6.8V
C100 Chip	6.7V	±0.15V	6.1 – 7.2V
D100 Chip	6.7V	±0.2V	6.0 – 7.2V
Temperature Coefficient	+2.5 mV/°C	±0.3 mV/°C	1.8 – 3.1 mV/°C

6. Schottky-Barrier Diodes (A100/B100/C100 Only)

PARAMETERS	TYPICAL VALUES	σ-LIMIT	WORST CASE TOLERANCE
Forward Voltage Drop @ 10 μA	0.36V	±0.02V	0.22 to 0.44V
Temperature Coefficient of Forward Voltage Drop	-1.5 mV/°C	±0.1 mV/°C	±0.3 mV/°C
Reverse Breakdown Voltage	30V	–	20 – 40V
Leakage Current @ 20V	200 nA	–	1 nA – 1 μA

7. Diffused Resistors (All Master Chips)

PARAMETERS	TYPICAL VALUES	σ-LIMIT	WORST CASE TOLERANCE
Absolute Values	–	±10%	±25%
Temperature Coefficients			
-55°C to -25°C	-650 ppm/°C	±100 ppm	–
-25°C to 0°C	+150 ppm/°C	± 40 ppm	–
0°C to 25°C	+680 ppm/°C	± 40 ppm	–
25°C to 75°C	+1040 ppm/°C	± 20 ppm	–
75°C to 125°C	+1400 ppm/°C	± 40 ppm	–
Matching Between Resistors			
Identical Values	–	±0.8%	±2.4%
Non-Identical Values			
200 – 450	–	±1.6%	±4.8%
200 – 900	–	±1.7%	±5.1%
200 – 1.8K	–	±1.9%	±5.7%
200 – 3.6K	–	±2.0%	±6.0%
450 – 900	–	±1.5%	±4.5%
450 – 1.8K	–	±1.7%	±5.1%
450 – 3.6K	–	±1.9%	±5.7%
900 – 1.8K	–	±1.5%	±4.5%
900 – 3.6K	–	±1.7%	±5.1%
1.8K – 3.6K	–	±1.5%	±4.5%

8. Pinch-Resistors

PARAMETERS	TYPICAL VALUES	σ-LIMIT	WORST CASE TOLERANCE
Absolute Value Tolerance	±50%	–	+100% to -80%
Matching Between Identical Resistors	±20%	–	–
Breakdown Voltage	6.4V	–	–
Temp. Coefficient	+6,000 ppm/°C	–	8,000 ppm/°C

Digital Semi-Custom Design

Integrated Injection Logic (I^2L) technology extends the capabilities of semi-custom design to high complexity digital or combined analog/digital systems. Exar has made this possible by the development of a family of I^2L Master Chips which combine a large number of I^2L gates and Schottky-bipolar transistors on the same chip. Similar to its bipolar counterpart, Exar's I^2L semi-custom program also utilizes partially fabricated silicon wafers which are then "customized" by the application of special mask patterns.

Exar's digital Master Chips utilize bipolar input/output (I/O) interface circuitry on the same chip, along with the high-density I^2L logic arrays. Thus, outwardly the I^2L semi-custom chip looks and performs exactly as a bipolar LSI chip, which can readily interface with TTL or MOS level signals. In other words, these gate-array Master Chips combine the high functional density advantages of I^2L technology with the interface and load-drive capability of the bipolar circuitry on the same IC. This feature makes it very convenient to "retro-fit" I^2L LSI designs into existing MOS or TTL type logic systems.

ACHIEVING HIGH COMPLEXITY

Traditionally, the application of semi-custom design technology to complex digital systems has been somewhat limited due to one key factor: to be economically feasible, a complex digital LSI circuit must achieve a high functional density on the chip (i.e., high-gate count per unit chip area). This requirement is not compatible with the random interconnection concept which is key to the semi-custom or Master Chip design technique. Exar's *new* approach to this age-old problem overcomes this limitation; and achieves packing densities approaching those of full custom digital LSI layout while still maintaining the low-cost and the quick turn-around attributes of semi-custom IC design. This is achieved by making use of unique layout and interconnection properties of I^2L gates, and by extending the customizing steps to additional mask layers, besides the metal-interconnection pattern.

Exar's I^2L Master Chips are customized by not one but *three* mask layers:

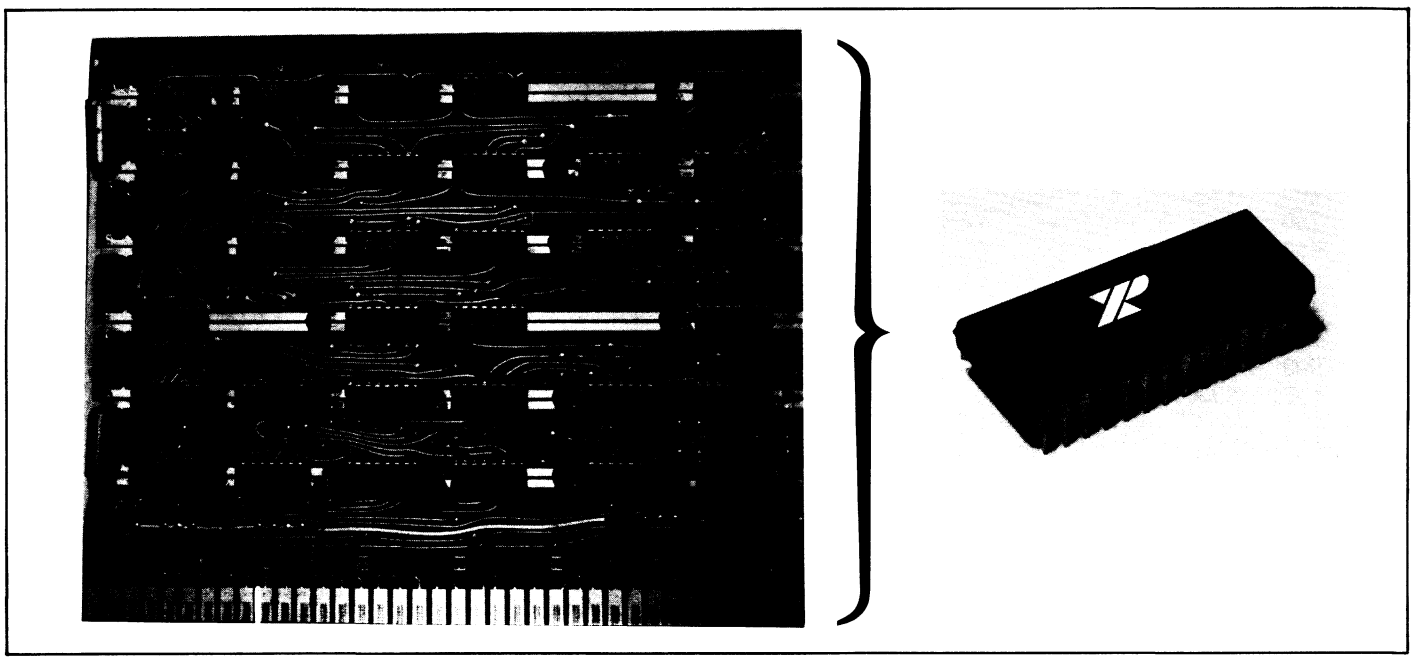
1. A custom diffusion pattern to define gate outputs and custom "underpasses" for interconnection.
2. A custom "contact" mask which opens contact windows or "activates" only those devices actually used in the design.
3. A custom metal interconnection mask which interconnects all the "activated" devices.

FULLY-AUTOMATED MASK GENERATION

Exar has developed a unique, fully-automated mask-generation technique which allows all three custom mask layers used with I^2L Master Chips to be generated simultaneously; directly from a customer's pencil layout on the Master Chip worksheet. This unique mask generation technique, and the *three-mask* customizing method are the heart of Exar's I^2L semi-custom program. In this manner, one is able to combine low-cost quick turn-around capabilities of semi-custom designs with the high functional density of I^2L technology, and make very efficient use of the chip area.

WHEN TO USE DIGITAL SEMI-CUSTOM

The key application of I^2L semi-custom design is to replace complex blocks of random-logic functions with a single monolithic chip. An entire digital sub-system comprised of many SSI or MSI chips, or discrete components can be put on a single I^2L Master Chip, thus providing significant cost and space savings and greatly improving system reliability. The availability of bipolar input-output interface circuitry on the same chip along with the high-density I^2L logic makes it very convenient to retrofit I^2L designs into existing MOS or TTL logic systems. Therefore semi-custom I^2L LSI designs provide cost-effective solutions for complex custom LSI requirements, even at production volumes as low as a few thousand pieces.



Features of I^2L Technology

Integrated Injection Logic (I^2L) is one of the most significant recent advances in the area of monolithic LSI technology. Compared to other monolithic LSI technologies, I^2L offers the following unique advantages.

High Functional Density: I^2L logic gates offer much smaller size than their bipolar counterparts. Thus, a much higher degree of logic complexity or functional density can be achieved on a given IC chip.

Easy to Interconnect: Unique structure and geometry of I^2L gates make them ideal for semi-custom design. An entire array of gates can be easily customized and interconnected with only three masks, without sacrificing high functional density.

Bipolar Compatible Processing: I^2L is a direct derivative of conventional bipolar IC technology. Therefore, one can combine bipolar devices on the same chip as I^2L gates. This feature has the following key advantages:

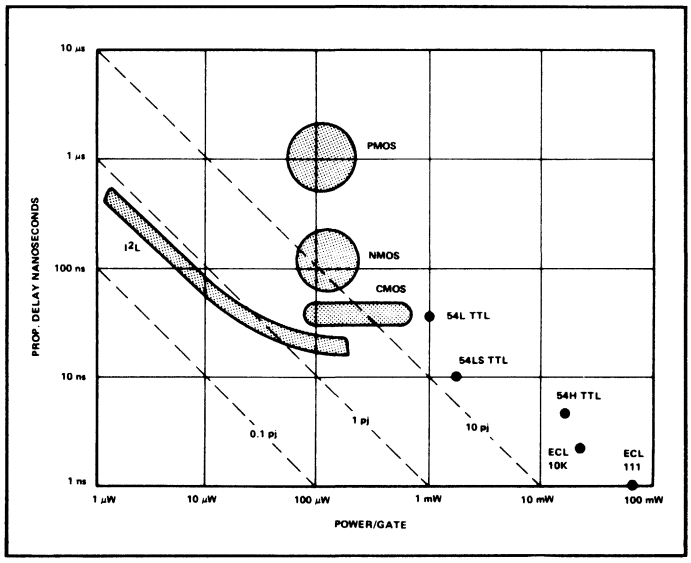
- Input-output sections of I^2L chips can be made bipolar. Thus, they can readily interface with existing logic families or retrofit into existing systems.
- Analog and digital functions can be combined on the same chip. One of Exar's Master Chips, the XR-400, is specifically designed for such an application.

Low-Voltage Operation: I^2L gates can operate with supply voltages as low as 1 volt, and require only a single power supply.

Low-Current and Low-Power Operation: Depending on speed requirements, I^2L gates can operate with current levels in the nano-Ampere range. This feature, along with its low-voltage operation makes it ideal for applications in low-power, battery operated systems.

Higher Reliability than MOS: Since I^2L gates have the same basic features of bipolar transistors, they are not subject to electrostatic burn-out problems associated with MOS transistors, and do not require special handling precautions.

Wide Operating Temperature: I^2L gates are not as affected by leakage currents as their MOS counterparts. Thus, they can be made to operate over the full military temperature range.



Comparison of Speed and Power Capabilities of Various Logic Families

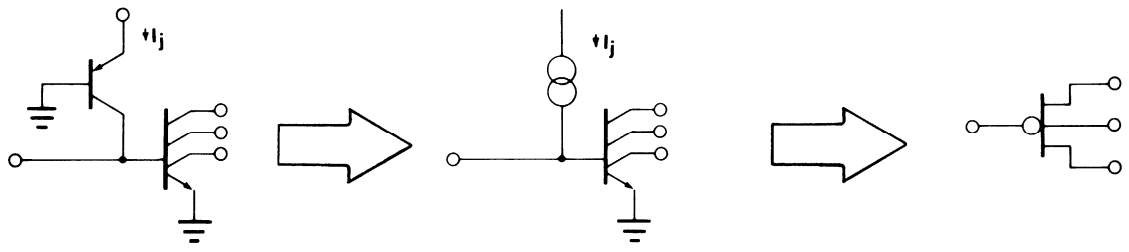
THE BASIC I^2L GATE

The I^2L logic technology is derived from the basic single-input, multiple-output inverter circuit shown below. The logic functions are performed in a manner similar to the case of conventional "open-collector" logic i.e., the outputs of various gates are interconnected together, in a wired-AND configuration. Most terminals of the I^2L gate share the same semiconductor region (for example, the collector of the PNP is the same as the base of the NPN; and the emitter of the NPN is the same as the base of the PNP). This leads to a very compact device structure which occupies very small chip area. As a result, the functional density of I^2L gates on a chip is comparable to that of MOS gates, and is approximately 5 times higher than conventional TTL logic.

LOGIC CONVERSION TO I^2L GATES

Converting conventional logic diagrams from their NAND/NOR gate equivalents to I^2L gates is a simple and straight-forward procedure. This information is contained in I^2L Design Manual, which is available as a part of Exar's I^2L Design Kit. In addition, Exar has developed a large "Library" of I^2L logic sub-blocks corresponding to popular logic functions, such as decoders, flip-flops and counters, which greatly simplifies this conversion process.

THE BASIC I^2L GATE



(a) Actual Gate (b) Equivalent Circuit (c) Logic Symbol

Designing with I^2L Master Chips

Exar currently has three I^2L Master Chips in production, with additional chips in development for future applications. These are the XR-300, XR-400 and the XR-500 Master Chips which combine bipolar transistors on the same chip along with I^2L gate arrays. The XR-300 and the XR-500 are mainly designed for digital systems; the XR-400 Master Chips is intended for systems requiring both analog and digital functions.

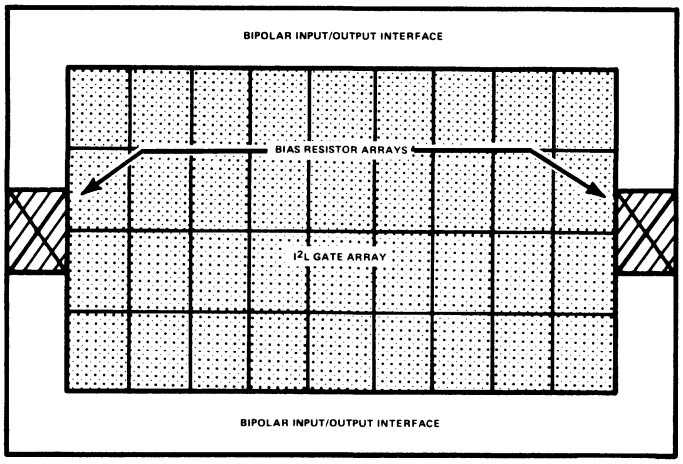
All three of these Master Chips are fabricated with the same manufacturing process. They differ only in their architecture and the number of components. All three of these chips are especially designed for Exar's unique *three-mask* customization process, using fully-automated mask generation techniques. Depending on the voltage breakdown requirements of the bipolar transistors, each of these chips are available with *two* options:

- **Option A: Maximum Operating Voltage of 6.0 volts.**
- **Option B: Maximum Operating Voltage of 12.0 volts.**

These options *only* effect the bipolar input/output interface sections of Master Chips, and have no effect on the performance characteristics of the I^2L gates.

XR-300 AND XR-500 MASTER CHIPS

These Master Chips are primarily designed for all-digital systems. They contain a large number of multiple-output I^2L gates along with Schottky-bipolar input/output buffers. Except for the difference in size, both chips have the same architecture shown below: the I^2L gates are arranged in array-form at the center of the chip, and the bipolar input/output buffers are located along the periphery of the chip. In addition, the bipolar I/O sections of both chips contain two identical sets of resistor arrays, located at opposite ends of the chip, which are used for biasing the injectors of the I^2L gates. The XR-300 chip contains 288 5-output I^2L gates and 28 I/O buffers. The XR-500 chip contains 520 5-output gates and 40 I/O Buffers. A detailed description of the bipolar input/output interface circuitry is given on Page 26.



Basic Layout of XR-300 and XR-500 Master Chips

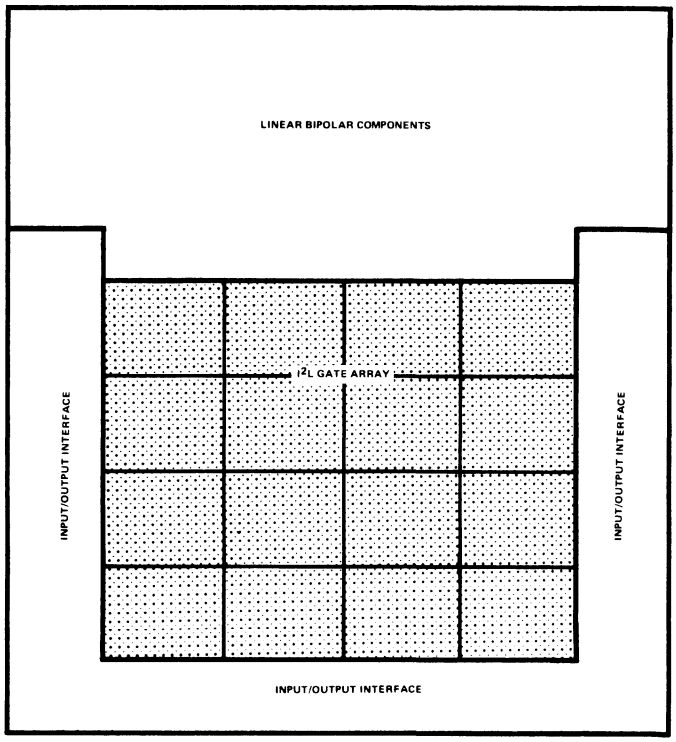
XR-400 MASTER CHIP

The XR-400 Master Chip is designed primarily for applications requiring the combination of analog and digital functions on the same chip. Thus, it is made up of both a linear and a digital section. The digital section of the chip has the same basic architecture as the XR-300: it contains 256 5-output I^2L gates and 18 Schottky-bipolar I/O interface sections. The linear section of the chip is made up of an array of NPN and PNP transistors and resistors, and is very similar to Exar's bipolar Master Chips.

COMPONENT UTILIZATION

The unique *three-mask* customizing technique used in Exar's I^2L Master Chips makes them very efficient for both ease of logic layout and component utilization. One of the three customizing mask steps is a "custom diffusion" step which allows one to place low-resistance "cross-unders" or under-passes selectively on the chip. This technique provides the designer with virtually two layers of interconnection on the chip, and thus greatly simplifies the logic layout and improves the component utilization efficiency. Normally, in the case of random combinational logic, one can easily utilize 60% to 80% of the total gates available on a given I^2L Master Chip. In the case of sequential and repetitive logic circuits, the gate utilization is normally as high as 80% to 100%.

In the case of the XR-400 Master Chip, which combines analog circuit components and the digital gates on the same chip, the *three-mask* customizing techniques is only applicable to the digital section. The analog section of the chip is customized with only the inital-interconnection pattern, similar to the case of linear Master Chips.



Basic Layout of XR-400 Master Chip

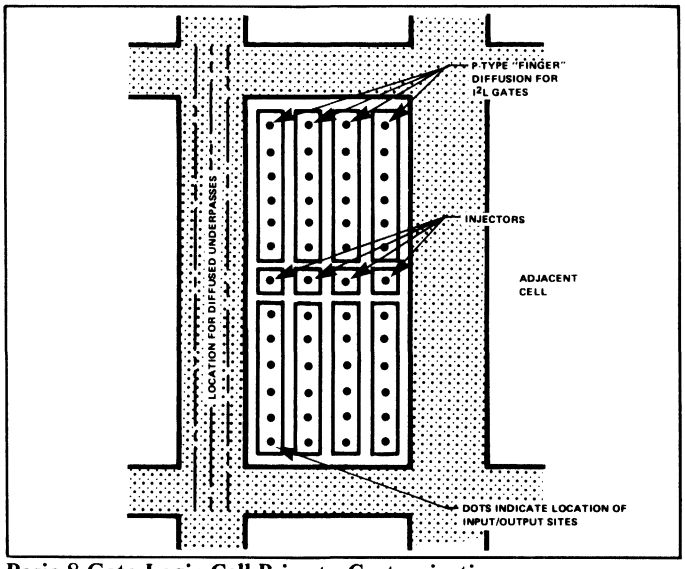
THE I^2L GATE ARRAY SECTION

This section of the I^2L Master Chips is made up of logic "cells" which contain a number of multiple-output I^2L inverters, grouped together. The figure below shows the typical layout of such a cell made up of eight multiple output inverters which share a common set of four injectors. The basic gate cells forming the I^2L gate array are made up of P-type injectors and P-type gate *fingers* which serve as the base regions of the I^2L gates. The six dots on each gate area indicate the possible locations or *sites* for gate input or outputs. The particular use of these sites as an input or an output is determined by two custom masks: an N-type collector diffusion mask which defines the locations of outputs, and a custom contact mask which opens the appropriate input and output contact. Finally, a third custom mask is applied to form the metal interconnections between the gates, and the gate cells. The custom N-type diffusion step, which determines the locations of gate outputs, is also used for forming low-resistivity underpasses between the gate-cells. The area between each of the gate cells can accommodate two or three parallel underpasses in the horizontal and the vertical direction, respectively. Since the N-type diffusion which forms these underpasses is a part of the customizing step, the location and the length of each underpass can be chosen to fit a given interconnection requirement. This method provides the designer with virtually all the advantages and capabilities of multi-layer interconnection paths on the surface of the chip; and allows approximately 80% of the gates on the chip to be utilized in a typical logic layout.

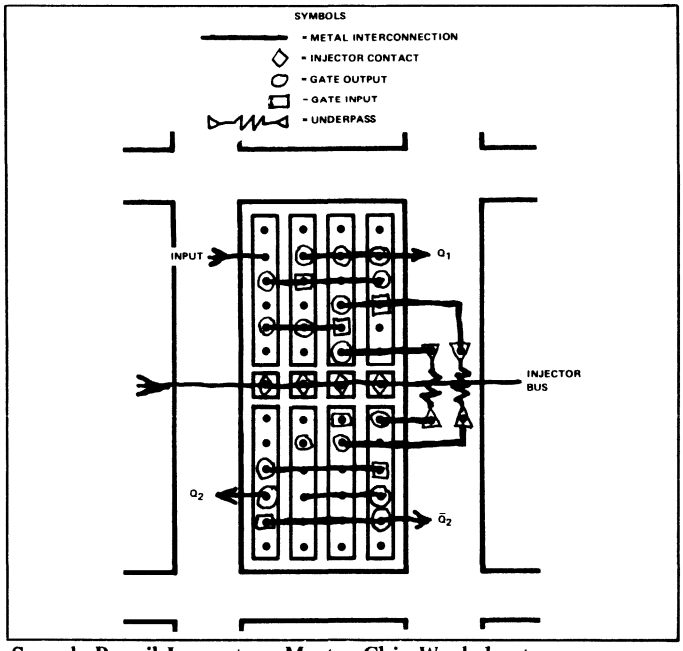
The custom logic interconnections can be easily laid out in pencil on a layout sheet by simply interconnecting the desired gate sites with a pencil line and appropriately defining the function of the site as an input, output, injector contact or an underpass. The function of each of the potential sites is defined by simply drawing an appropriate symbol on it, such as a circle for an "output" and a square for an "input," as defined in the example below.

COMPONENTS AVAILABLE ON I^2L MASTER CHIPS

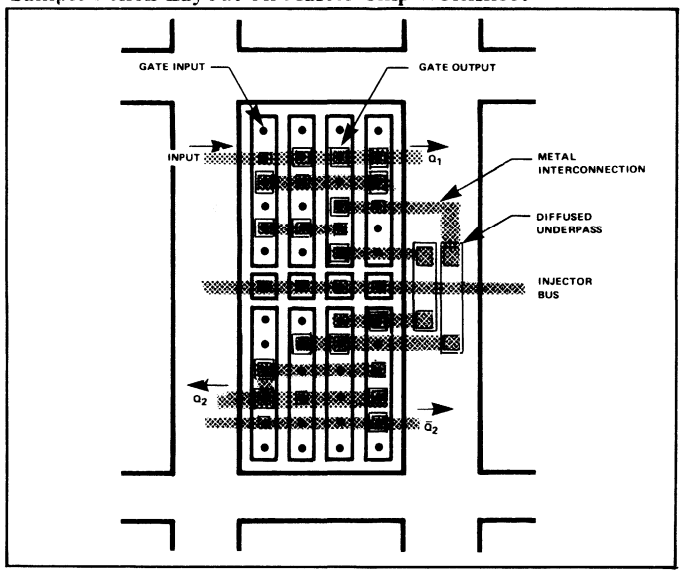
CHARACTERISTIC	CHIP TYPE		
	XR-300	XR-400	XR-500
I^2L Gates	288	256	520
Schottky-Bipolar I/O Interfaces	28	18	40
Max. Operating Voltage			
A-Option	6V	6V	6V
B-Option	12V	12V	12V
Available Bonding Pads	34	40	42
Linear Components			
NPN Transistors	-	45	-
4-Collector PNP's	-	12	-
Diffused Resistors	-	336	-
Pinch Resistors	-	8	-
Chip Size (mils)	106 x 144	119 x 156	122 x 185



Basic 8-Gate Logic Cell Prior to Customization



Sample Pencil Layout on Master Chip Worksheet

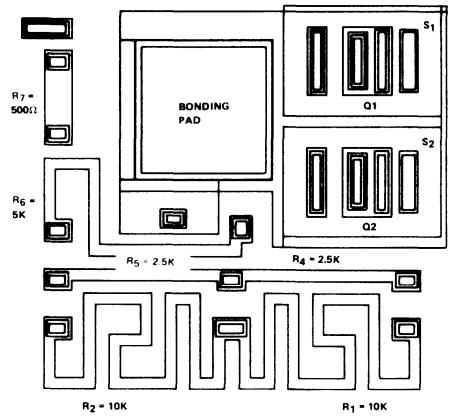


Sample Layout of 8-Gate Cell After Customizing it with N+ Collector Diffusion, Contact Mask and Metal Interconnection Pattern

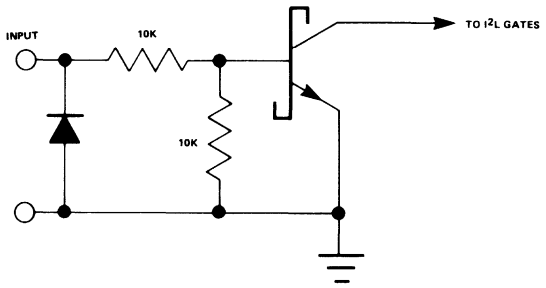
BIPOLAR INPUT/OUTPUT INTERFACE SECTION

The bipolar input/output interface sections of the I^2L Master Chips are located along the periphery of the chips. The component locations in a typical I/O cell are shown in the adjacent figure. Each I/O cell is designed to be either an "input" or an "output" interface, depending on the choice of the metal interconnection pattern applied to the cell. Furthermore, two adjacent cells can be combined together, to provide tri-state type output buffer. Some of the basic input and output circuit configurations available from the I/O interface are shown below. In the case of a tri-state output configuration, one would also utilize several gates from the I^2L logic section, to perform the necessary gating functions.

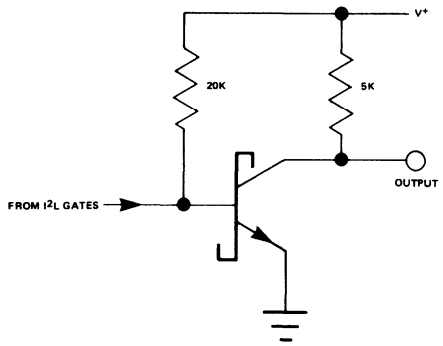
Each input/output interface cell contains one bonding-pad, several resistors of varying values, a clamp-diode to substrate and two NPN transistors with optional Schottky-diode clamps. Each NPN transistor is capable of sinking 5mA of current with Schottky-diode clamps, and 10mA of current without Schottky-diode clamps, at a saturation voltage of $\leq$0.5V. The break-down-voltage of the bipolar I/O section is $\geq$6V and $\geq$12V, respectively, for "Option A" and "Option B" versions of the I^2L Master Chips.



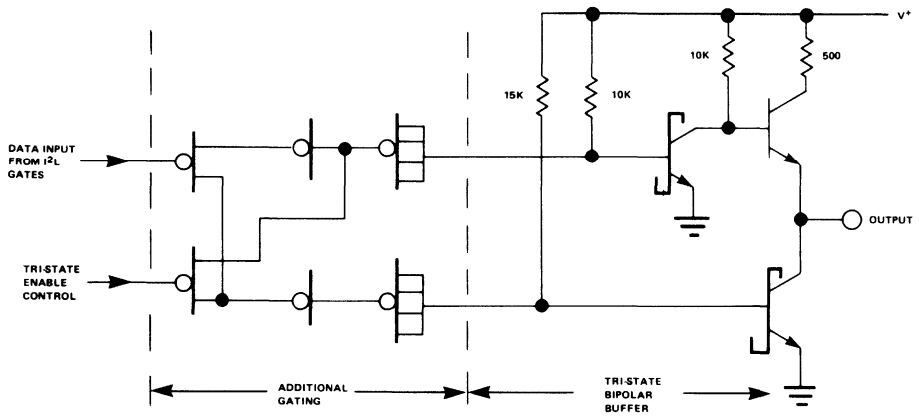
A Typical Schottky-Bipolar Input/Output Interface Cell



(a) Input Interface Circuit



(b) Output Interface Circuit



(c) Tri-State Output Interface Circuit

Typical Bipolar Input/Output Interface Circuits Available from I/O Interface Cell

XR-300 I^2L Master Chip

Chip Size: 104 x 140 mils
(2.6 x 3.5 mm)

5-Output I^2L Gates: 288

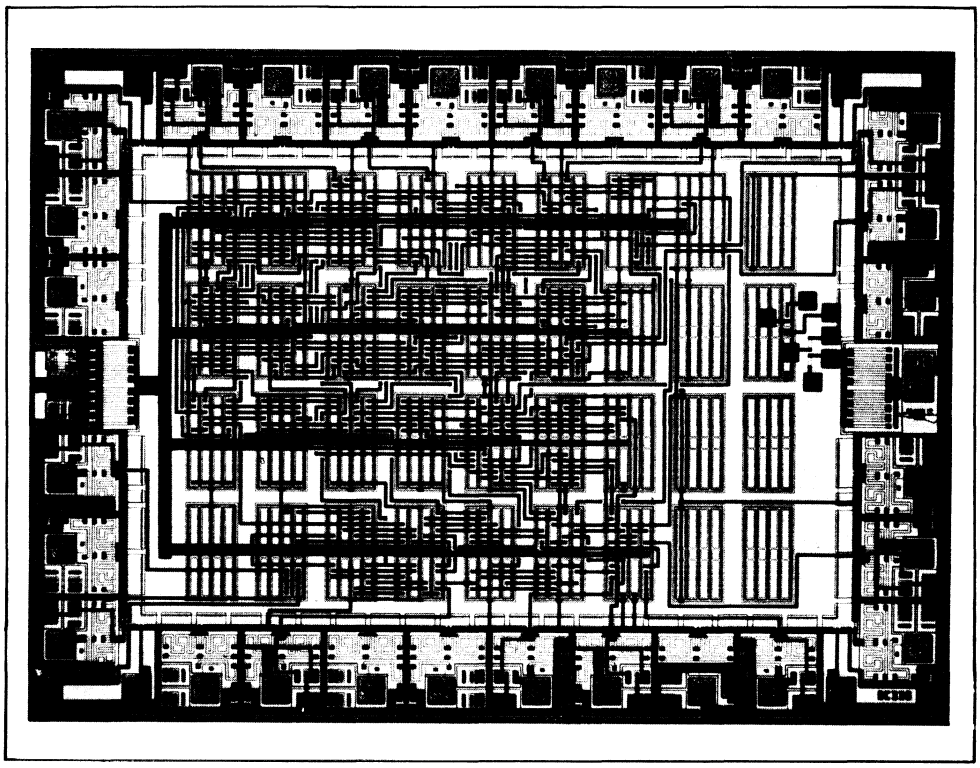
Schottky-Bipolar I/O Interfaces: 28

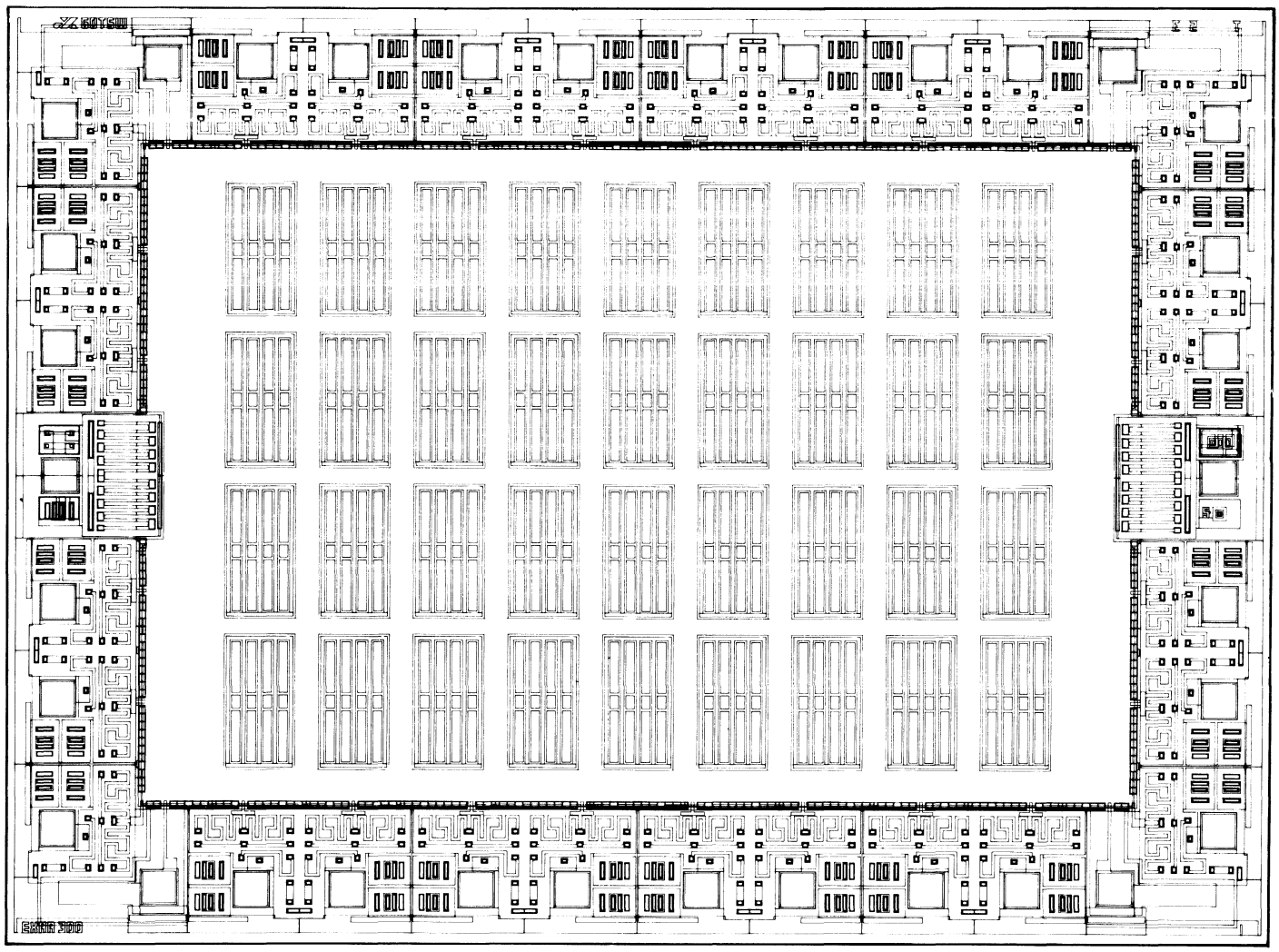
Bonding Pads: 34

Max. Operating Voltage:

Option A: 6V

Option B: 12V





XR-400 I^2L Master Chip

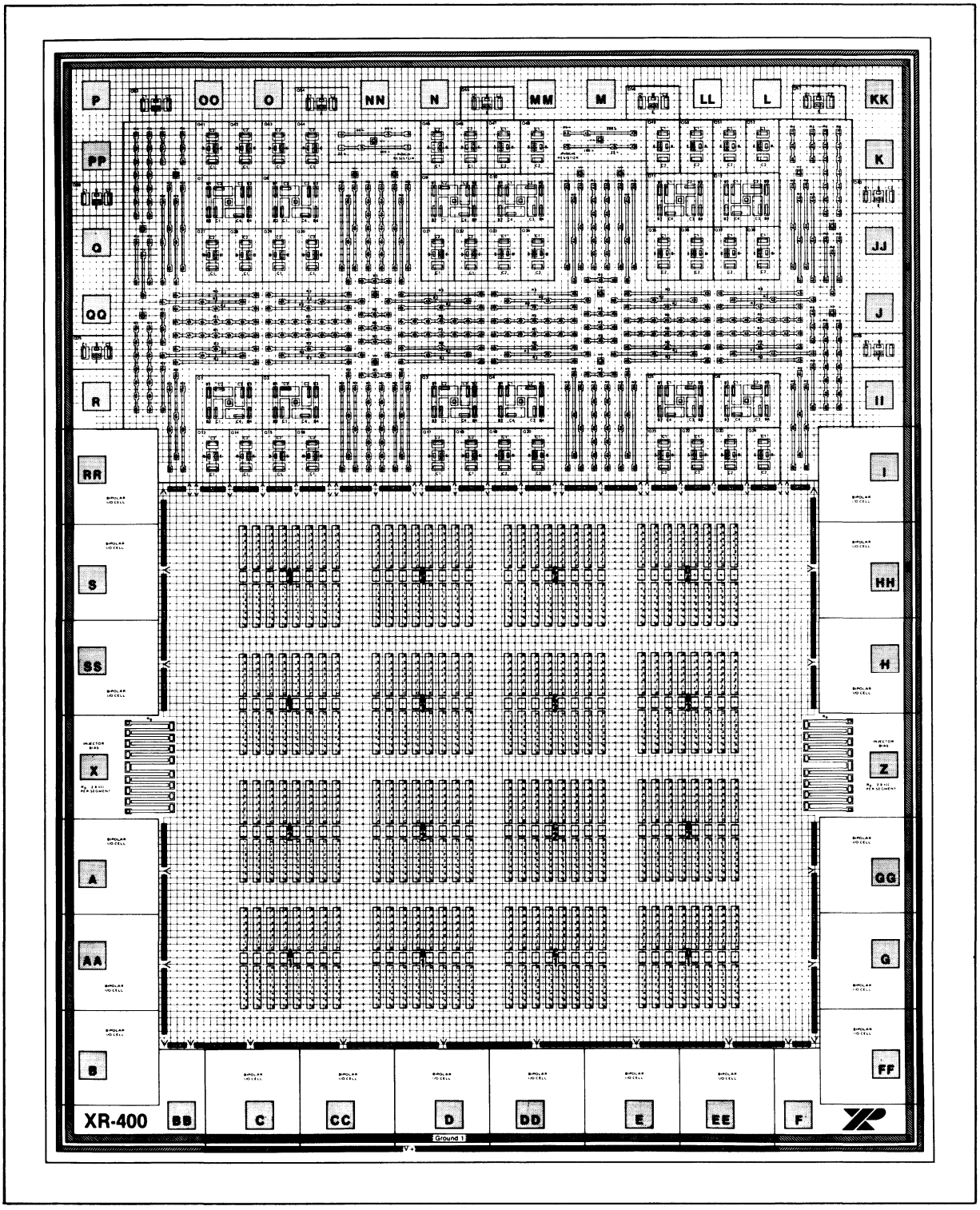
Digital Components:

5-Output I^2L Gates: 256
Schottky-Bipolar I/O Interfaces: 18
Bonding Pads: 40
Max. Operating Voltage:
  Option A: 6 V
  Option B: 12 V

Linear Components:

NPN Transistors: 45
4-Collector PNP Transistors: 12
Diffused Resistors:
  700 Ω: 200
  2.5 kΩ: 116
  5kΩ: 20
Pinch Resistors: (Option B Only)
  25 kΩ: 4
  100 kΩ: 4

Chip Size: 119 x 156 mils
(3.02 x 3.96 mm)



XR-500 I^2L Master Chip

Chip Size: 122 x 185 mils
(3.1 x 4.6 mm)

5-Output I^2L Gates: 520

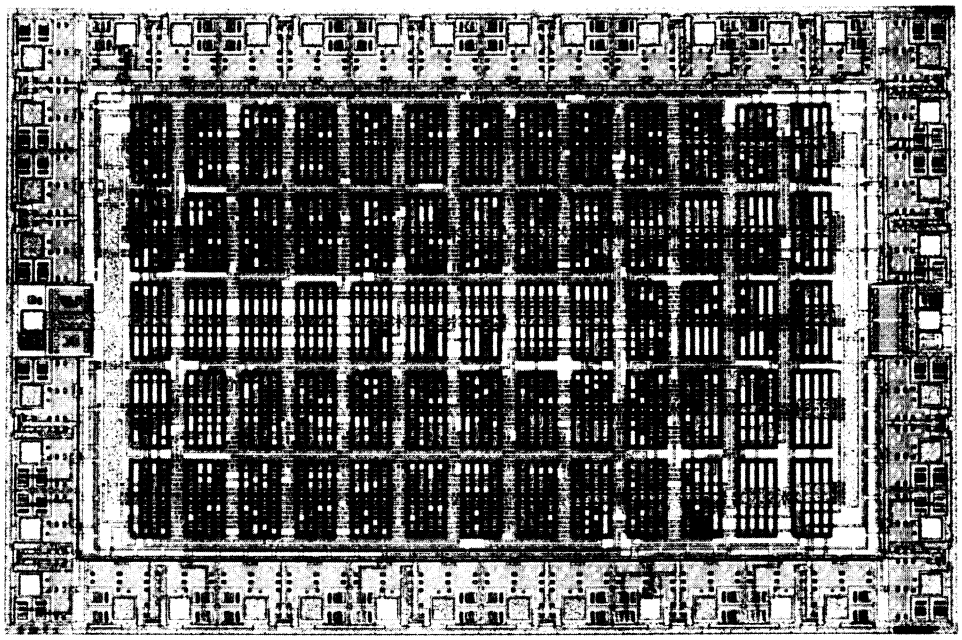
Schottky-Bipolar I/O Interfaces: 40

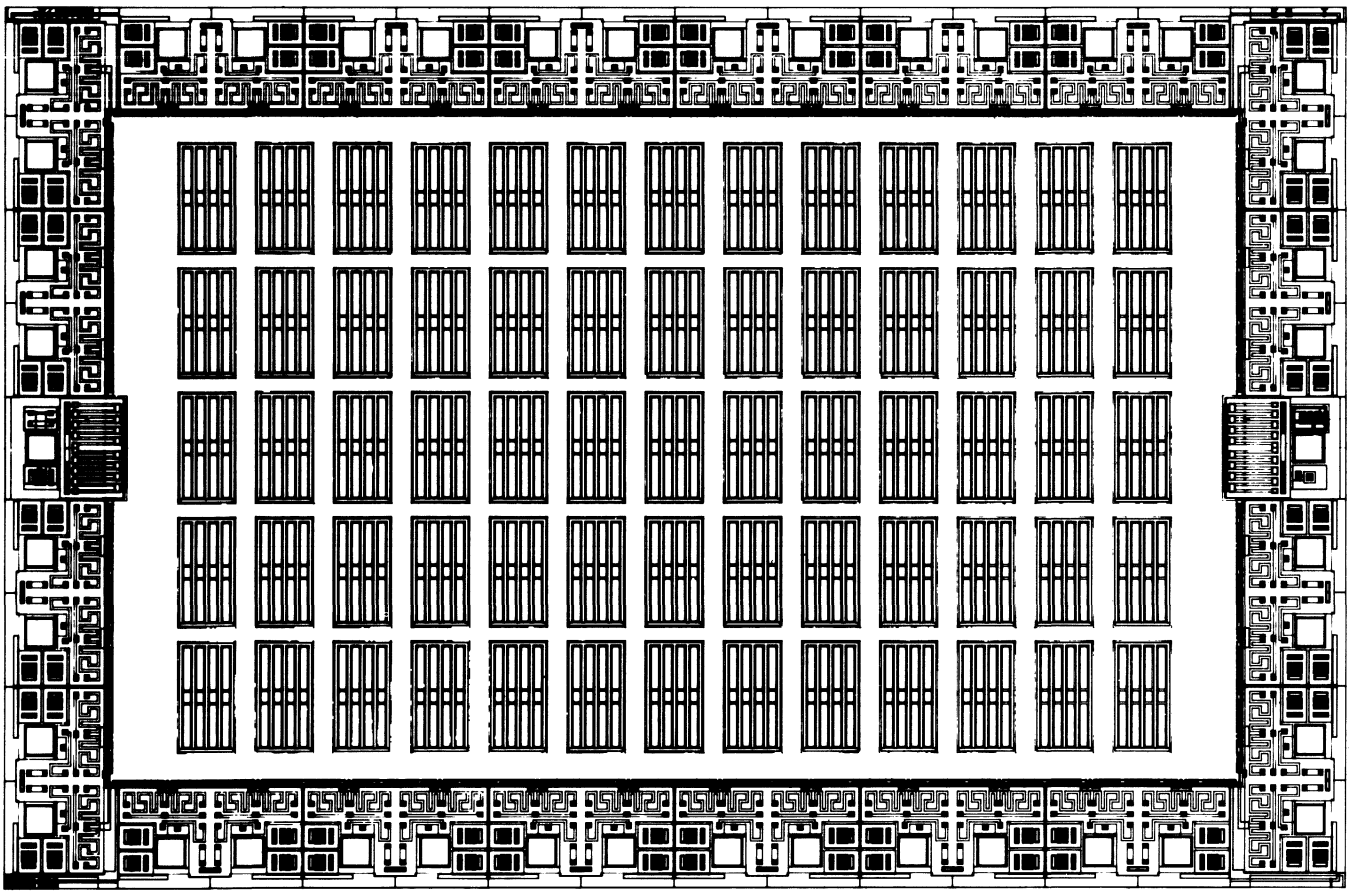
Bonding Pads: 42

Max. Operating Voltage:

Option A: 6V

Option B: 12V

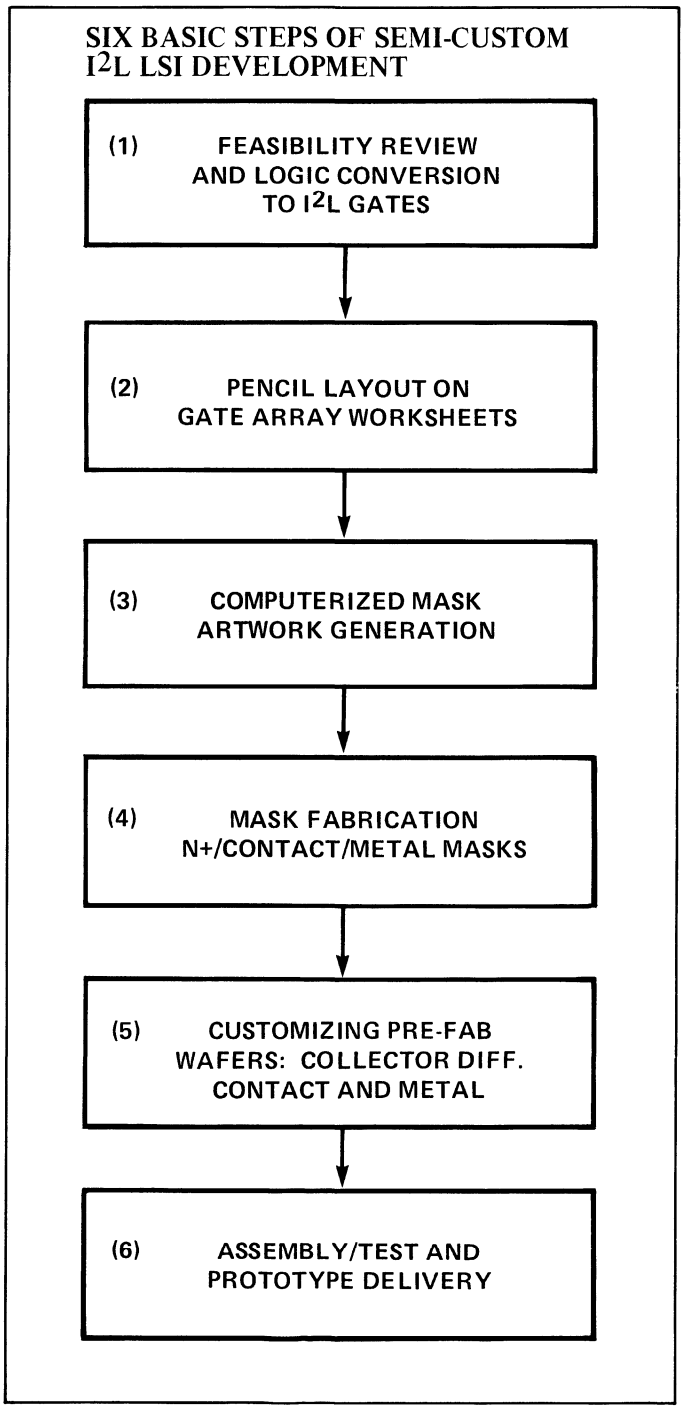




Digital Semi-Custom Design Cycle

The digital semi-custom LSI design program using Exar's I^2L Master Chips is devised for maximum versatility and flexibility, to suit varying customer needs and capabilities. The flow-chart below gives the outline and the sequence of *six* basic steps associated with a typical I^2L semi-custom program.

In many cases, the *first two steps* indicated in the flow-chart can be done by the customer, in consultation with Exar, using Exar's I^2L Design Kit and the design instruction manual. Whenever possible, such an approach is recommended, since it greatly reduces the development costs and the turnaround time.



STEP 1. FEASIBILITY REVIEW AND LOGIC CONVERSION

Starting with the customer's logic diagram (preferably reduced to flip-flops and gates) the first step is a detailed review of the system requirements with regards to the overall gate count, I/O requirements, operating speeds, etc., to assure feasibility of integration, and to choose the most economical gate array chip to be used. If the results of this review indicate feasibility, the next step is to convert the logic diagram into I^2L gates. At this state, a computer simulation of the logic diagram may also be performed, if deemed necessary.

STEP 2. PENCIL LAYOUT ON GATE ARRAY WORKSHEETS

Once the logic diagram is converted to I^2L gates, the next step will be to make a pencil layout of the circuit on the appropriate array worksheet. This pencil layout is done on a blank worksheet where the gate input and output locations are shown as target dots (see page 25). During the layout, an appropriate symbol is placed over the corresponding dot on the gate outline, and the interconnections and the underpasses between the gates are indicated by pencil lines and with appropriate symbols. In this layout, the bipolar I/O cells do not need to be internally interconnected. Since these cells are standardized, it is only necessary for the designer to specify if a particular I/O cell is to be used as an input or an output.

STEP 3. COMPUTERIZED MASK ARTWORK GENERATION

Using a specially developed computerized mask generation technique, the three layers of necessary custom IC tooling (i.e., for custom N-type diffusion, contact window cut; and the metal interconnections) can be automatically generated by a single "digitizing" step from the pencil layout. This simultaneous and automated generation of the three custom mask layers greatly reduces the tooling cost and turnaround time, and avoids mask errors.

STEP 4. MASK FABRICATION

The photographic tooling plates, or "masks," are fabricated by a pattern-generation technique from the digitized coordinate information stored in the computer.

STEP 5. CUSTOMIZING PREFABRICATED WAFERS

The prefabricated I^2L wafers containing the P-type base diffusion and the gate "fingers" are customized into completed monolithic LSI chips using the custom IC tooling generated in Steps 3 and 4.

STEP 6. ASSEMBLY/TEST AND PROTOTYPE DELIVERY

The completed monolithic chips are first evaluated on the finished IC wafer, and later assembled, electrically tested and delivered as the completed prototypes. The amount of electrical testing done on the initial prototypes depends on customer's specific needs and requirements.

Exar's Digital Semi-Custom Programs

Exar offers two digital semi-custom development programs, using the I^2L Master Chips:

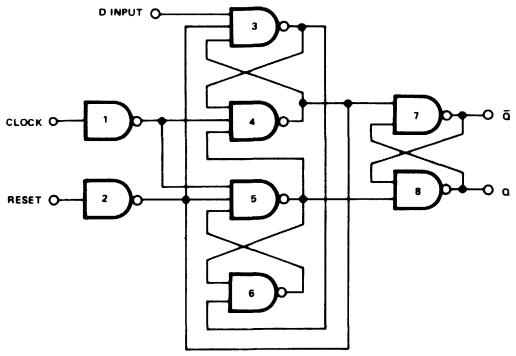
PROGRAM A: *Exar Does Entire Design Starting From Customer's Logic Diagram:* Starting with customer's logic diagram, Exar proceeds to generate necessary IC layout and tooling; and fabricates the IC prototypes.

PROGRAM B: *Customer Does His Own Design Using I^2L Design Kit:* Using the I^2L Kit and the Design Manual, the customer can do his own breadboarding and pencil layout of his system on the Master Chip layout forms. Exar reviews this layout; generate necessary tooling and fabricates the IC prototypes.

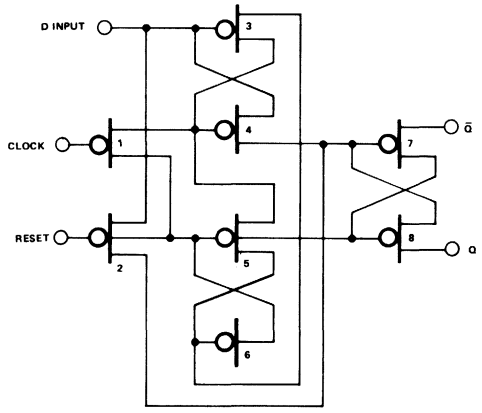
PROGRAM A	PROGRAM B
EXAR DOES DESIGN FROM CUSTOMER'S LOGIC DIAGRAM *(All Steps Performed by Exar)*	CUSTOMER DOES DESIGN AND LAYOUT USING I^2L DESIGN KIT *(Steps 1 and 2 Performed by Customer)*
(1) REVIEW CUSTOMER'S LOGIC DIAGRAM	(1) BREADBOARD EVAL. USING I^2L KIT
(2) LOGIC CONVERSION TO I^2L	(2) GENERATE CIRCUIT LAYOUT ON MASTER CHIP LAYOUT FORMS
(3) CIRCUIT LAYOUT ON MASTER CHIP	(3) SUBMIT LAYOUT TO EXAR FOR REVIEW
(4) GENERATION OF IC TOOLING	(4) EXAR GENERATES IC TOOLING
(5) IC WAFER FABRICATION	(5) EXAR FABRICATES IC WAFERS
(6) PROTOTYPE IC ASSEMBLY	(6) EXAR ASSEMBLES IC PROTOTYPES

DESIGN EXAMPLE

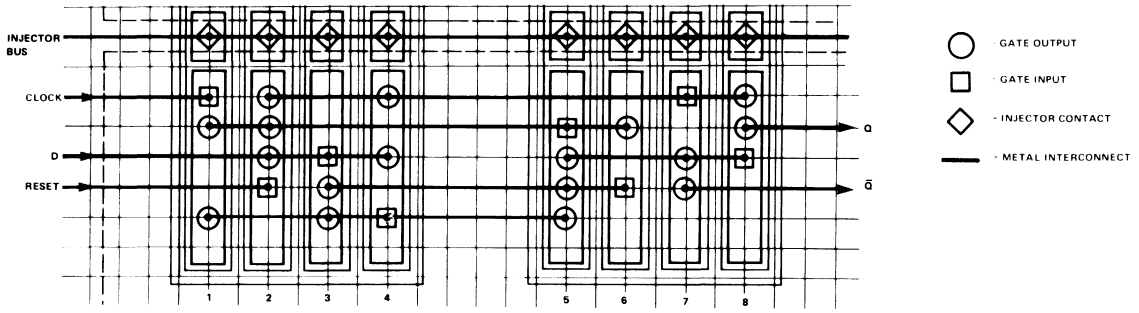
The multiple-output I^2L gates on the Exar's Master Chips are arranged in 8-gate "cells." A complex logic array can be partitioned into sub-sections, and each of these sub-sections can be laid out on one or more of these cells. The example below shows the layout of a D-type flip-flop in one of Exar's Master Chips. The dark lines in the layout example correspond to the metal interconnection busses; the circles and squares indicate the respective gate outputs and inputs. As a part of the I^2L Design Kit, Exar supplies a complete Design Manual and special layout worksheets which enable the customer to do his own logic-conversion and layout.



(a) Nand Logic Diagram

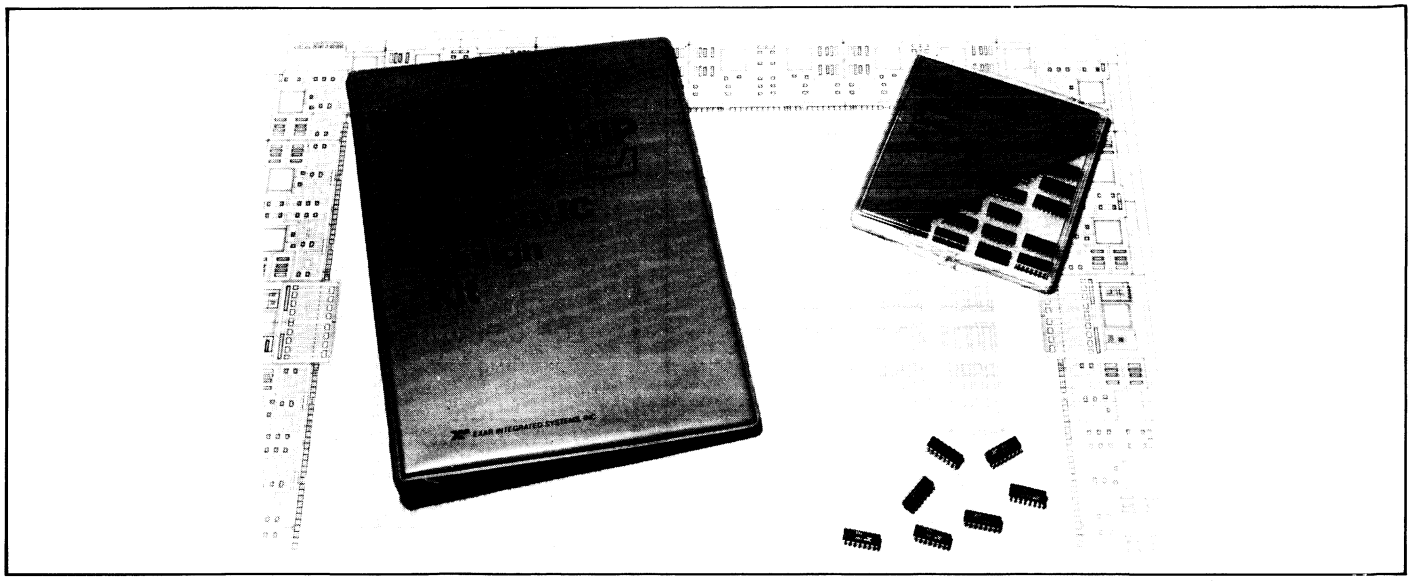


(b) I^2L Gate Diagram



(c) Typical Pencil Layout on Master Chip Worksheet

I^2L Design Kit



Exar's I^2L Design Kit provides an ideal vehicle for the customer to familiarize himself with the fundamentals of I^2L logic and then proceed to do the design and the layout of his own semi-custom I^2L LSI chip. This Design Kit contains the following:

- A set of 40 monolithic "kit parts" for system design and breadboarding.
- A comprehensive "Design Manual" which covers the fundamentals of I^2L logic and provides design and layout examples.
- A set of layout worksheets which lets the user prepare his own logic layout directly on the I^2L Master Chip.

The monolithic kit parts which make up the I^2L Design Kit are comprised of basic logic building blocks such as gate-arrays, latches and flip-flops as well as bipolar input/output buffers. The kit parts allow the designer to breadboard and characterize his circuit performance, and optimize his design, well in advance of performing the final circuit layout. In this manner, the problems and pitfalls normally encountered in converting a discrete logic system into a monolithic design are avoided. In addition, the kit also includes a special I^2L evaluation or test chip, the XR-C409. This test circuit contains frequency-dividers and ring-oscillators to evaluate the high frequency capabilities and the power-speed trade-offs of I^2L gates.

The I^2L Design Manual gives a comprehensive review of I^2L logic technology and describes the electrical characteristics of each type of component available in the Master Chips. It also presents some of the anticipated parameter distribution and the "worst-case" tolerances associated with each type of circuit component. In addition, the Design Manual also provides a "library" of I^2L-equivalents of logic sub-blocks corresponding to popular logic functions such as decoders, flip-flops, counters and multiplexers and gives layout examples which demonstrate the efficient use of layout worksheets.

ADDITIONAL KIT PARTS

The amount of kit parts supplied as a part of the I^2L Design Kit are sufficient for most designs. However, if additional kit parts are required to complete your evaluation, these can be obtained either directly from Exar, or through your local Exar technical representative.

TECHNICAL ASSISTANCE

If any special or unusual circuit design or layout problems are encountered in the preparation of your semi-custom IC layout Exar's technical staff will be glad to review your design problem and provide technical guidance. In many cases, it is beneficial to call Exar for a preliminary discussion of your custom IC needs, even before you decide to buy a Design Kit.

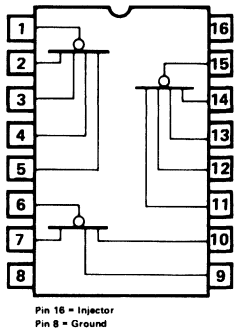
COMPONENTS INCLUDED IN I^2L DESIGN KIT

PART NUMBER	DESCRIPTION	QUANTITY
XR-C501	I^2L Triple Inverter Array	15
XR-C502	Quad NOR-Gate Array	4
XR-C503	Dual D-type Flip-Flop (unbuffered)	8
XR-C504	Dual D-type Flip-Flop with Bipolar I/O Buffers	2
XR-C505	Dual J-K Flip-Flop (unbuffered)	4
XR-C506	I^2L Compatible NPN Transistor Array	4
XR-C507	I^2L Compatible PNP Transistor Array	2
XR-C409	I^2L Evaluation Circuit	1
	Total	40

Components in I^2L Design Kit

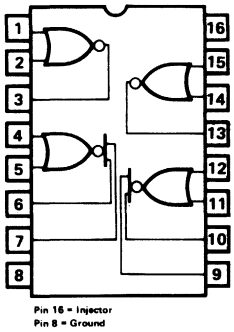
NOTE: When breadboarding with I^2L kit parts included in the Design Kit, a word of caution is in order: The high-frequency capabilities of I^2L gates in the kit which have unbuffered outputs are to a large extent limited by the parasitic capacitances associated with the package or the external wiring on the circuit board. In the monolithic design, when the electrical connections are made internal to the chip and the outputs are buffered, these parasitic package capacitances do not present a problem. However, when breadboarding with I^2L kit parts which have no buffered outputs, these package capacitances may limit the switching speeds obtainable at the kit-part breadboard stage.

XR-C501
I^2L INVERTER ARRAY



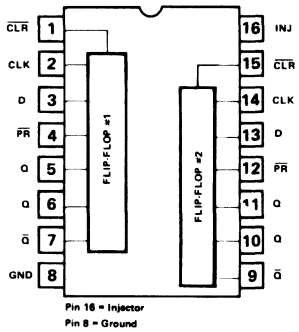
XR-C501 contains three multiple-output I^2L inverters. These three gates each have independent inputs and outputs, however they share a common injector.

XR-C502
I^2L NOR-GATE ARRAY



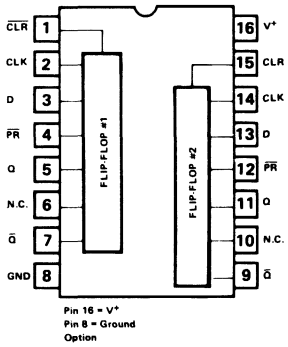
XR-C502 contains two single- and two dual-output I^2L NOR gates. All four gates share a common injector.

XR-C503
DUAL "D" FLIP-FLOP



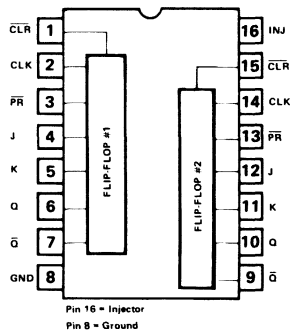
XR-C503 contains two independent D-type flip-flops. Both flip-flops share a common injector and trigger on negative-going edges. Both the inputs and the outputs of each flip-flop are unbuffered.

XR-C504
BUFFERED DUAL-D FLIP-FLOP



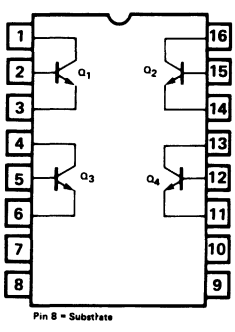
XR-C504 is a "buffered" version of the XR-C503 flip-flop array. Both flip-flops contain Schottky-bipolar input and output buffers (see page 26). The two flip-flops share a common injector which is internally connected to V^+ terminal. With $V^+ = 5V$, the I^2L gates are biased at approximately 50 μA/gate.

XR-C505
DUAL J-K FLIP-FLOP



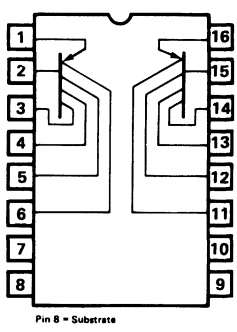
XR-C505 contains two independent J-K flip-flops which share a common injector. Both the inputs and outputs are comprised of unbuffered I^2L gates.

XR-C506
I^2L COMPATIBLE NPN TRANSISTOR ARRAY



XR-C506 contains four small-signal NPN transistors. These are equivalent to the transistors available in the linear section of the XR-400 Master Chip.

XR-C507
I^2L COMPATIBLE PNP TRANSISTOR ARRAY

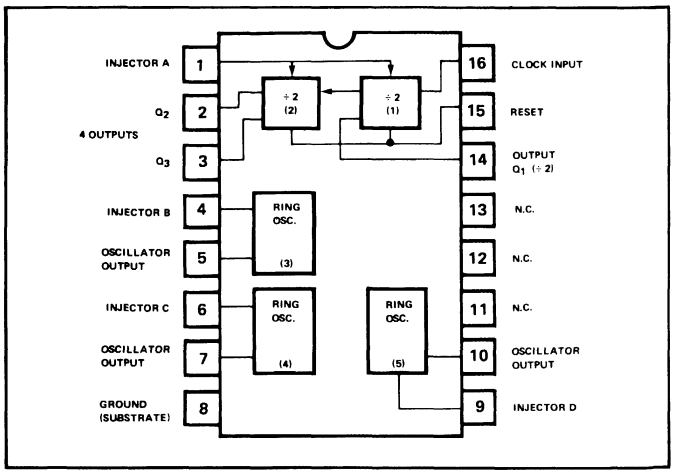


XR-C507 contains two four-collector lateral PNP transistors. These devices are equivalent to the PNP transistors available in the linear section of the XR-400 Master Chip.

XR-C409 I^2L Evaluation Circuit

The XR-C409 monolithic IC is a test circuit for evaluation of speed and performance capabilities of Exar's Integrated Injection Logic (I^2L) technology. It is intended to familiarize the I^2L user and the digital system designer with some of the performance features of I^2L, such as its high-frequency capability and power-speed tradeoffs.

The XR-C409 I^2L test circuit is comprised of five separate evaluation blocks as shown in the figure. Blocks 1 and 2 are D-type flip-flops which are internally connected as frequency dividers. Each of these dividers provide buffered open-collector outputs. Blocks 3, 4, and 5 are 8-stage ring-oscillators with buffered outputs to be used for measuring gate propagation delays at different injector current levels. The XR-C409 evaluation circuit is included as a part of Exar's I^2L Design Kit.



Electrical Characteristics of I^2L Master Chip Components

I^2L GATES (All Master Chips)

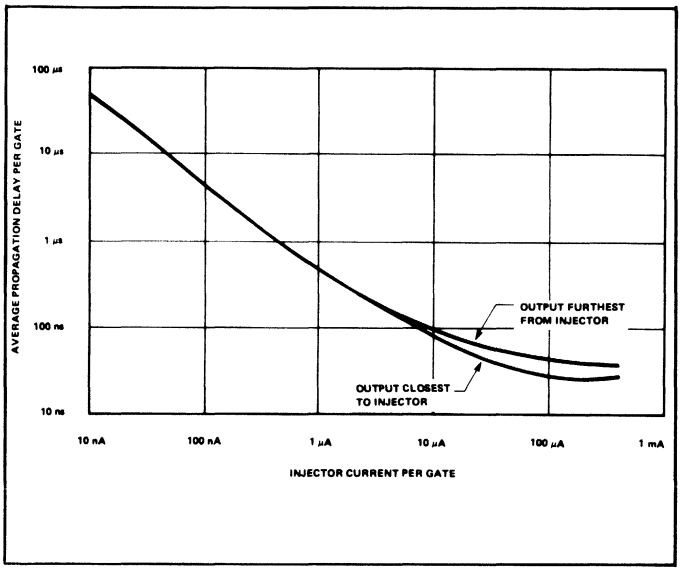
PARAMETER	TYPICAL CHARACTERISTICS AT VARIOUS INJECTOR CURRENTS			
	I_j = 100nA	I_j = 1μA	I_j = 10μA	I_j = 100μA
Output Sink Current, I_O	300 nA	8 μA	80 μA	600 μA
Output Sat. Voltage, V_{OL}	3mV	3mV	4mV	10mV
Input Threshold	0.48V	0.54V	0.60V	0.66V
Power-Delay Product (V^+ = 1V)	0.6 pJ	0.6 pJ	1.0 pJ	3 pJ
Average Prop. Delay	6 μsec	0.6 μsec	100 nsec	50 nsec
Max. Toggle Freq. (D F/F)	6 kHz	60 kHz	400 kHz	2 MHz
Input OFF Current (V_{IN} = 0)	150 nA	1.5 μA	15 μA	130 μA
Output Breakdown Voltage (Unbuffered Output)	3V	3V	3V	3V

SMALL SIGNAL NPN TRANSISTORS (Linear Section of XR-400 Chip Only)

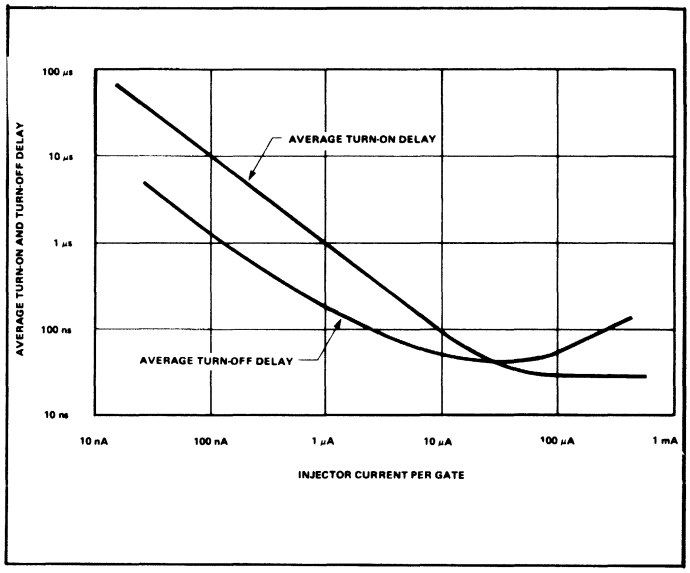
PARAMETER	TEST CONDITION	TYPICAL VALUES	SIGMA LIMIT	WORST CASE TOLERANCE
Current Gain (h_{FE})	I_C = 1 mA, V_{CE} =	200	–	80 – 800
Temp. Coefficiency of h_{FE}	–55°C to +25°C	+0.5%/°C	–	–
	25°C to 125°C	+1%/°C		
Matching of h_{FE}	I_C = 1 mA	–	±5%	±20%
Breakdown Voltage	LV_{CEO}			
Option A		8V		6 – 10V
Option B		15V		15 – 20V
Cutoff Frequency (f_T)	I_C = 1 mA	500 MHz		
Saturation Resistance		50 Ω		30 – 100 Ω

LATERAL PNP TRANSISTORS (Linear Section of XR-400 Only)

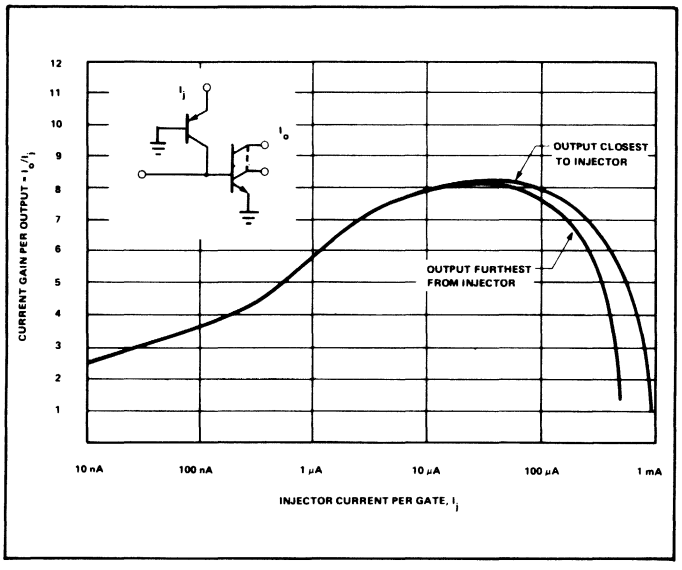
PARAMETER	TEST CONDITION	TYPICAL VALUES	SIGMA LIMIT	WORST CASE TOLERANCE
Current Gain (h_{FE})	I_C = 100 μA	10		5 – 20
(All collectors shorted)	I_C = 10 μA	30		10 – 50
Temp. Coefficiency of h_{FE}	I_C = 10 μA	±0.1%/°C		
Matching of h_{FE}	I_C = 10 μA	±3%	±5%	
Breakdown Voltage	LV_{CEO}	25V		15 – 30V
Cutoff Frequency (fT)	I_C = 100 μA	5 MHz		



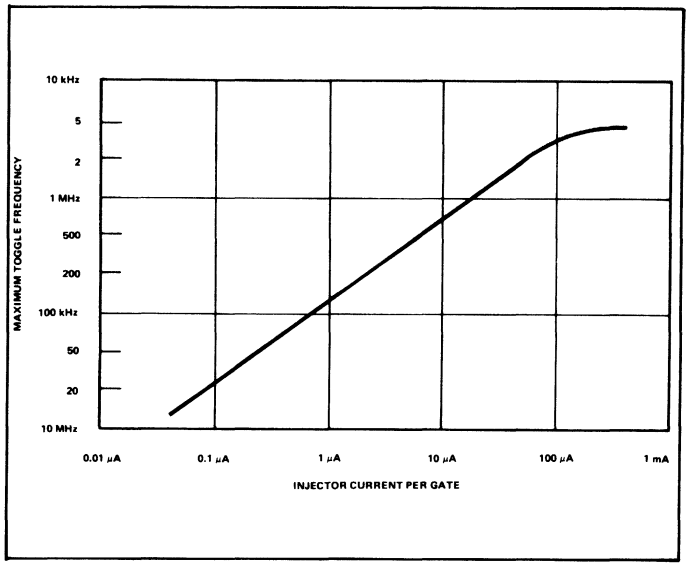
Propagation Delay Characteristics of I^2L Gates as a Function of Injector Current.



Average Turn-On and Turn-Off Delay vs. Injector Current.



Composite Current Gain as a Function of Injector Current. *(Note: Composite gain is defined as the ratio of maximum output current to injector current.)*

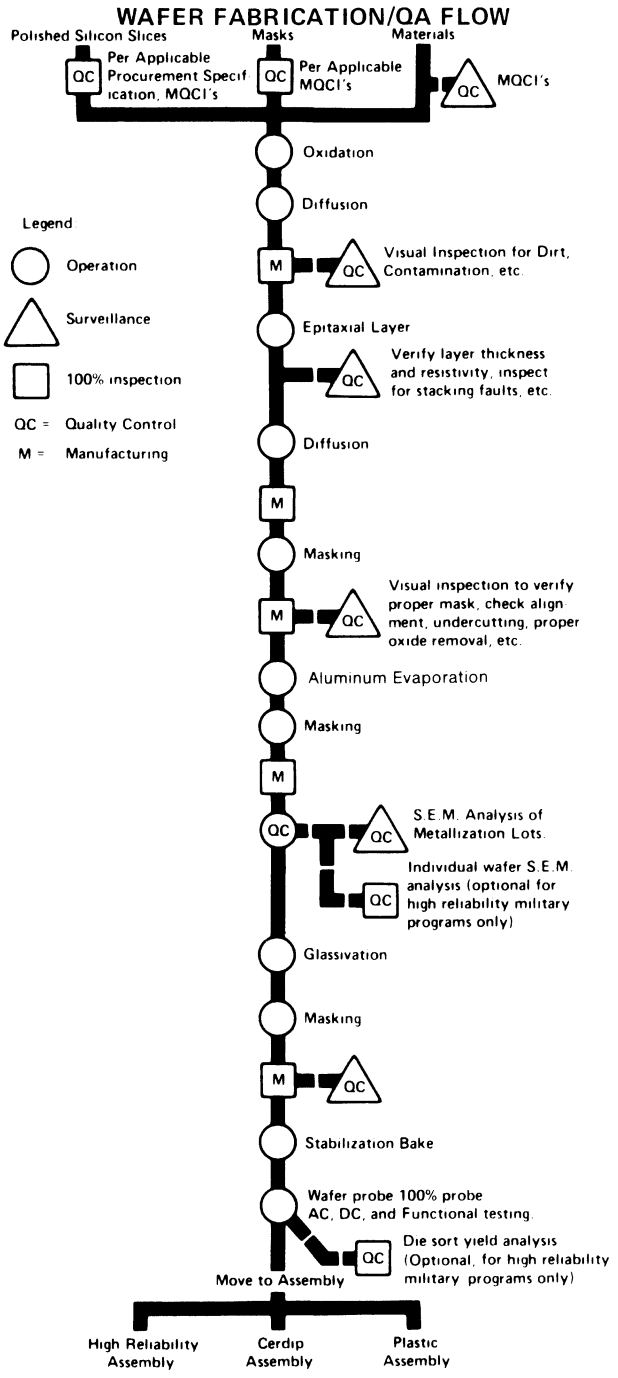


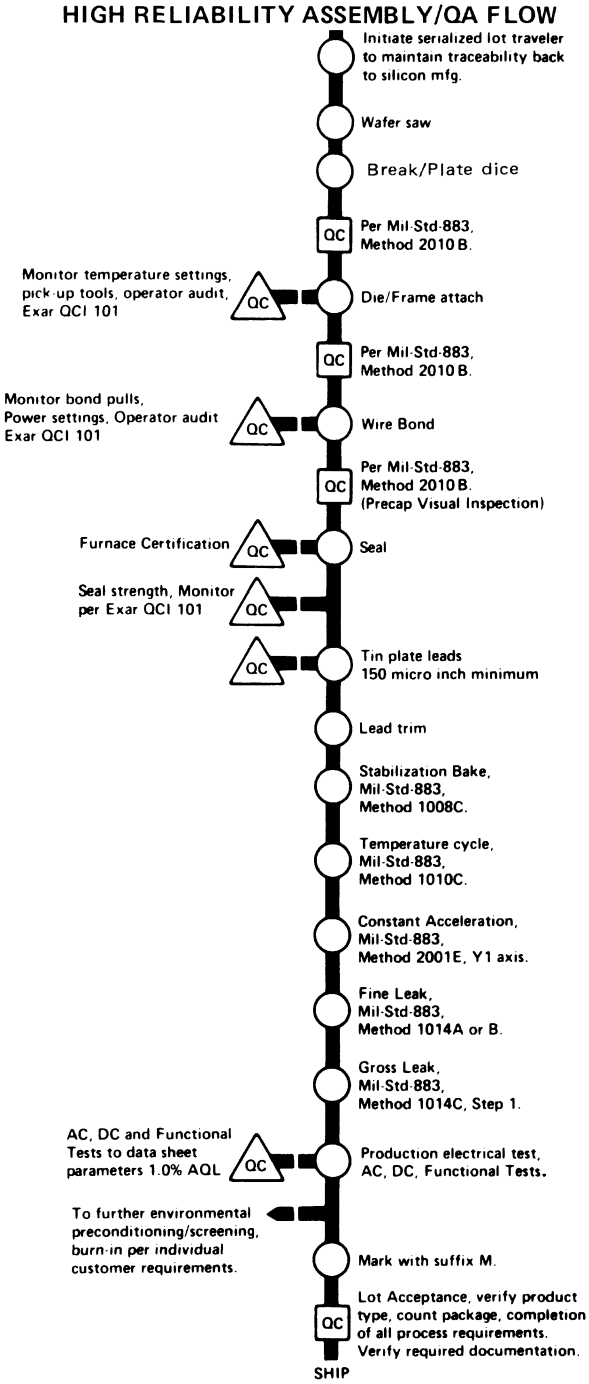
Maximum Toggle Rate of D-Type Flip-Flop as a Function of Injector Current.

Quality Assurance Standards

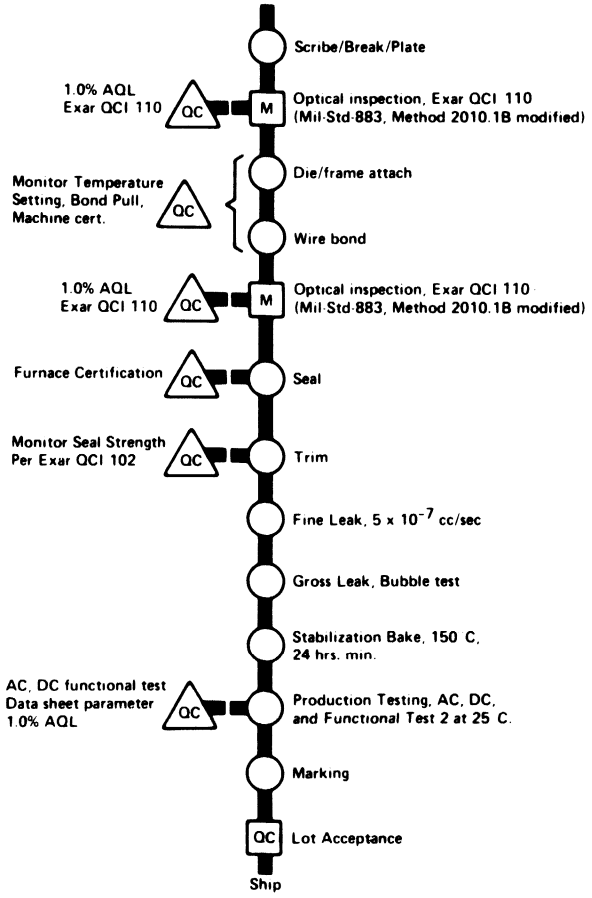
The quality assurance program at Exar Integrated Systems defines and establishes standards and controls on manufacturing, and audits product quality at critical points during manufacturing. The accompanying Manufacturing/QA process flows illustrate where quality assurance audits, by inspection or test, the manufacturing process. The insertion of these quality assurance points is designed to insure the highest quality standards are maintained on Exar product during its manufacture.

Realizing that these standard Manufacturing/QA process flows do not meet the needs of every customer's specific requirements, Exar quality assurance can negotiate and will screen product to meet any individual customer's specific requirement.

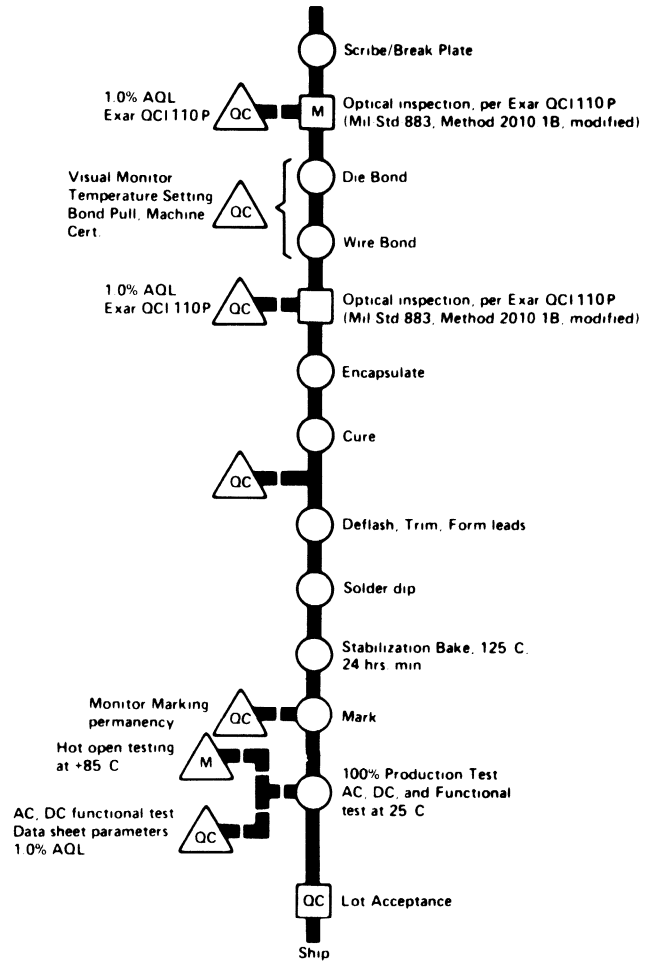




CERDIP ASSEMBLY/QA FLOW

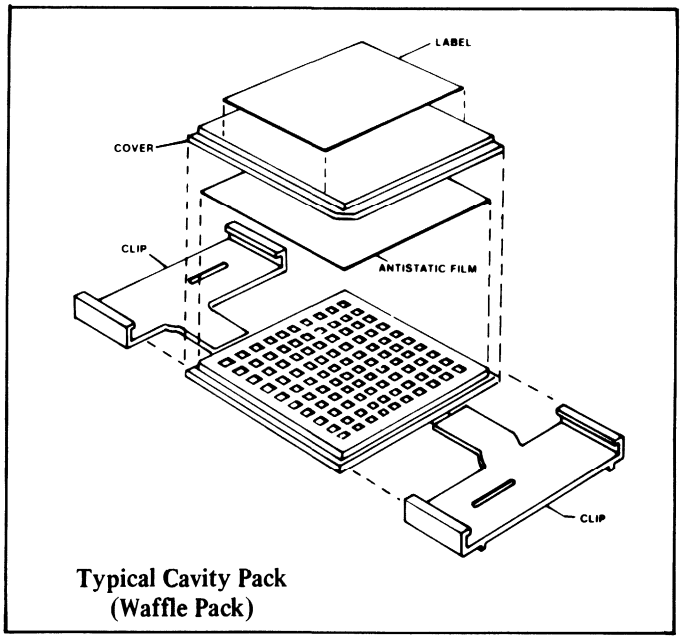


PLASTIC ASSEMBLY/QA FLOW



Monolithic Chips for Hybrid Assemblies

All of Exar's semi-custom IC products are also available in chip form. All chips are 100% electrically tested for guaranteed DC parameters at 25°C; and 100% visually inspected at 30x to 100x magnification using Exar's standard visual inspection criteria or MIL-STD-883 Method 2001, depending on the individual customer requirements. Each chip is protected with an inert glass passivation layer over the metal interconnections. The chips are packaged in waffle-pack carriers with an anti-static shield and cushioning strip plated over the active surface to assure protection during shipment. All chips are produced on the same well-proven production lines that produce Exar's standard encapsulated devices. The Quality Assurance testing of dice is provided by normal production testing of packaged devices.



Typical Cavity Pack (Waffle Pack)

HANDLING PRECAUTIONS AND PACKAGING OPTIONS

Extreme care must be used in the handling of unencapsulated semiconductor chips or dice to avoid damage to the chip surface. Exar offers the following three handling or packaging options for monolithic chips supplied to the customer:

Cavity or Waffle Pack: The dice are placed in individual compartments of the waffle pack (see figure). The plastic snap clips permit inspection and resealing.

Vial Pack: The vial is filled with inert freon TF and a plastic cap seals the vial. The freon acts as a motion retarder and cleansing agent.

Wafer Pack: The entire wafer is sandwiched between two pieces of mylar and vacuum sealed in a plastic envelope.